General Standards Corporation
High Performance Bus Interface Solutions

Rev: 062521

PMC66-24DSI6LN4AO

24-BIT PMC ANALOG I/O MODULE,

with

Six Low-Noise 24-Bit Analog Input Channels,

Four Precision 16-Bit Analog Output Channels,

10-Bit Digital I/O Port

REFERENCE MANUAL

--- PRELIMINARY ---

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC66-24DSI6LN4AO module provides six channels of 24-bit low-noise analog input capability in a single-width PMC module at sample rates up to 200 KSPS per channel. In addition, Four 16-bit analog output channels are accessed through individual registers. The module is functionally and mechanically compatible with PCI Specification 2.3, with 66 MHZ or 33 MHz bus and D32 read/write transactions. Power requirements consist of +5 VDC in accordance with the PCI specification, and operation over the specified temperature range is achieved with minimal air cooling.

All system input and output connections are made through a 68-Pin dual-ribbon cable connector. Figure 1.1 represents the physical configuration of the module. Specific details pertaining to performance are contained in the PMC66-24DSI6LN4AO product specification.

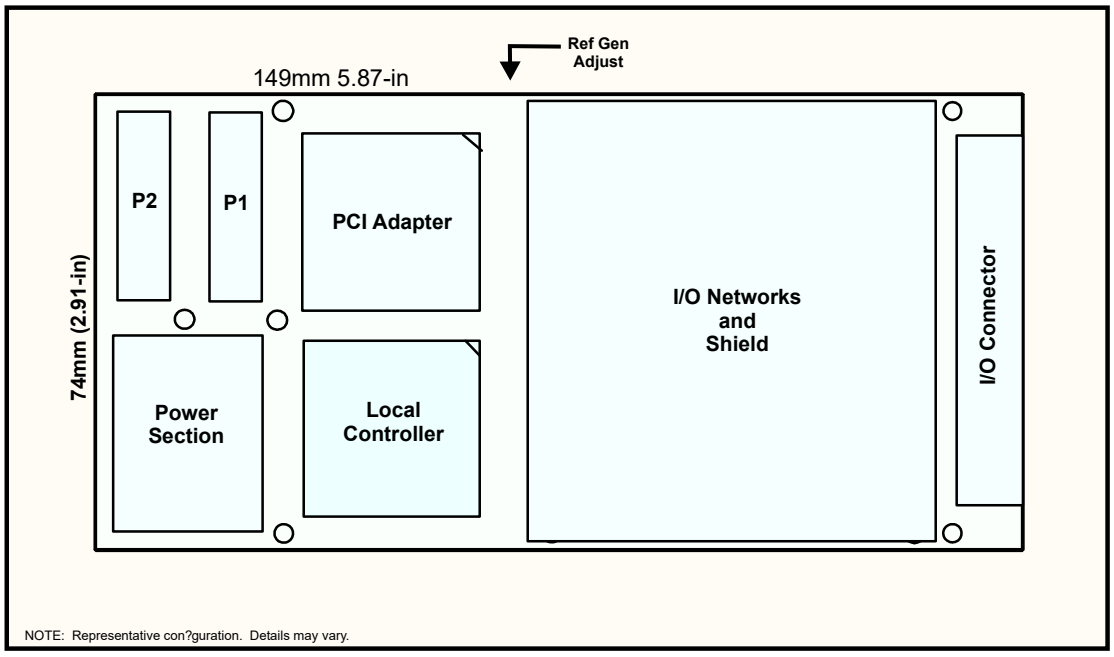

Figure 1.1. Physical Configuration

1.2 Functional Overview

A PCI interface adapter provides the interface between the controlling bus and the internal local controller through a 32-bit local bus (Figure 1.2). Inputs consist of six 24-Bit DSI ADCs, with one ADC dedicated to each input channel.

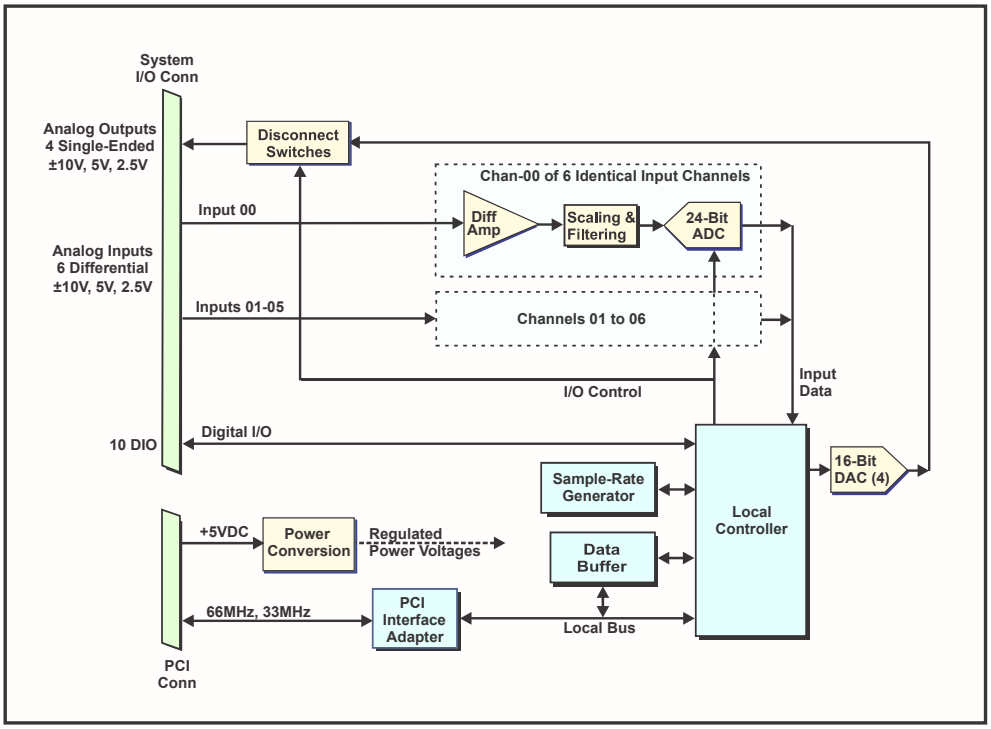

Figure 1.2. Functional Organization

An internal sample-rate clock generator is adjustable from 25.6 MHz to 51.2 MHz, and is divided down within the local controller to provide sample rates from 2.0 KSPS to 200 KSPS. Input bandwidth extends down to DC. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample FIFO data buffer. All input channels on a single board can be synchronized to perform sampling in phase-locked operation from a common clock.

Four analog output channels can be clocked either internally with either a rate generator or software, or externally by a hardware strobe. A self-clocking mode (Sequential) also is available. Each output channel contains a dedicated 16-Bit DAC.

A Digital I/O port provides eight bidirectional TTL pins, plus an uncommitted input and uncommitted output. All analog inputs and outputs are calibrated to a single precision internal reference voltage that can be monitored and adjusted through the I/O connector.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping package. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping package, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping package, position the board with the two PCI connectors facing the mating connectors J1, J2 on the host board (Figure 2.2-1). Then carefully press the board into position on the host. Verify that the mezzanine connectors have mated completely and that the board is seated firmly against the host board. Attach the board to the host with 2.5 x 6.5mm panhead screws. Pass the screws through the host board into the corresponding mounting holes in the standoffs and front-panel bezel. Tighten the screws carefully to complete the installation. Do not overtighten.

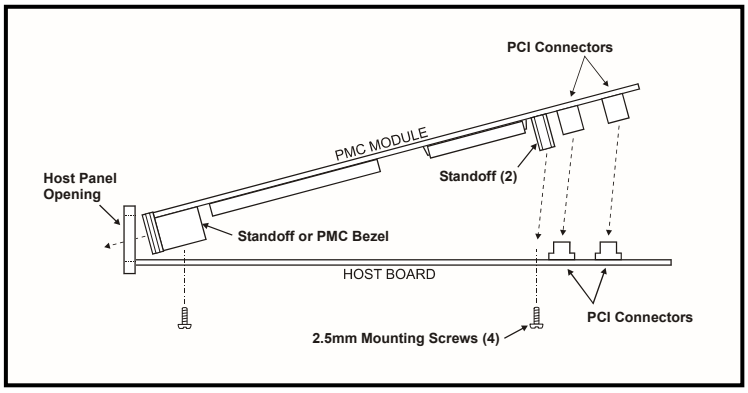

Figure 2.2.1. Mechanical Installation

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.1. The I/O connector is designed to mate with a 68-pin dual-ribbon connector equivalent to AMP #749621-7. The AMP insulation-displacement connector accepts two 34-wire 0.050-inch ribbon cables, with the pin assignments shown in Table 2.2.1 and in Figure 2.2.2. Contact the factory if preassembled cables are required.

Table 2.2.1 System Connector Pin Assignments

P5A	
PIN	SIGNAL
1	OUTPUT RETURN
2	OUTPUT CHANNEL 00
3	OUTPUT RETURN
4	OUTPUT CHANNEL 01
5	OUTPUT RETURN
6	OUTPUT CHANNEL 02
7	OUTPUT RETURN
8	OUTPUT CHANNEL 03
9	INPUT RETURN
10	INPUT RETURN
11	INPUT CHANNEL 00 LO (-)
12	INPUT CHANNEL 00 HI (+)
13	INPUT CHANNEL 01 LO (-)
14	INPUT CHANNEL 01 HI (+)
15	INPUT CHANNEL 02 LO (-)
16	INPUT CHANNEL 02 HI (+)
17	INPUT CHANNEL 03 LO (-)
18	INPUT CHANNEL 03 HI (+)
19	INPUT CHANNEL 04 LO (-)
20	INPUT CHANNEL 04 HI (+)
21	INPUT CHANNEL 05 LO (-)
22	INPUT CHANNEL 05 HI (+)
23	NO CONN*
24	NO CONN*
25	NO CONN*
26	NO CONN*
27	VREF RETURN
28	VREF ADJUST REFERENCE
29	VREF RETURN
30	VREF REMOTE ADJUST
31	VREF RETURN
32	RANGE VREF
33	VREF RETURN
34	VREF RETURN

P5B	
PIN	SIGNAL
1	DIGITAL RETURN
2	INPUT TRIGGER
3	DIGITAL RETURN
4	INPUT TRIGGER READY
5	DIGITAL RETURN
6	OUTPUT STROBE
7	DIGITAL RETURN
8	OUTPUT STROBE READY
9	DIGITAL RETURN
10	I/O DATA 00
11	DIGITAL RETURN
12	I/O DATA 01
13	DIGITAL RETURN
14	I/O DATA 02
15	DIGITAL RETURN
16	I/O DATA 03
17	DIGITAL RETURN
18	I/O DATA 04
19	DIGITAL RETURN
20	I/O DATA 05
21	DIGITAL RETURN
22	I/O DATA 06
23	DIGITAL RETURN
24	I/O DATA 07
25	DIGITAL RETURN
26	I/O CONTROL INPUT
27	DIGITAL RETURN
28	I/O CONTROL OUTPUT
29	DIGITAL RETURN
30	DIGITAL RETURN
31	DIGITAL RETURN
32	DIGITAL RETURN
33	DIGITAL RETURN
34	DIGITAL RETURN

*** Open circuit. No internal connection.**

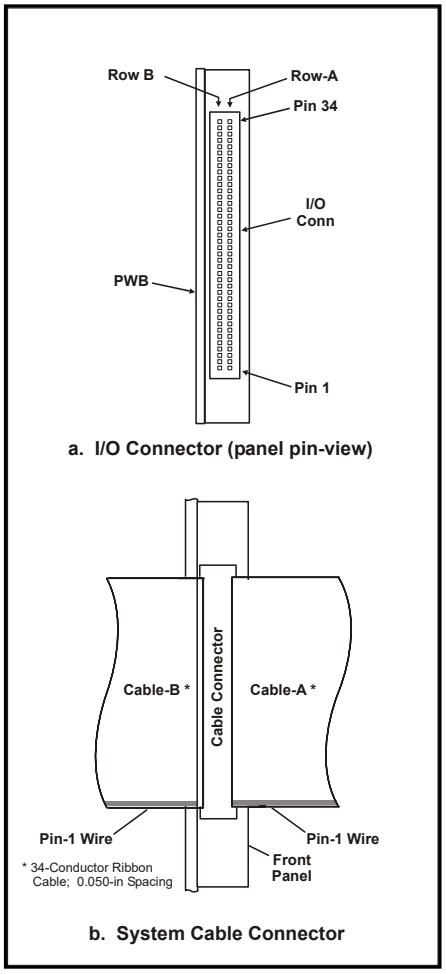

Figure 2.2.2. System I/O Connector

System Cable Mating Connector:
68-pin 0.050" Subminiature connector: with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:** Amp # 787170-7

2.3 Analog Input Configuration

The analog inputs can be software-configured as six differential input pairs or six single-ended input lines. All inputs are AC-Coupled to produce the best noise performance. Differential operation provides the highest noise immunity, and is recommended for the majority of applications. Pull-down resistors are provided on all analog inputs.

2.3.1 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1b, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return should be connected to system ground (remote common) as closely as possible to the input sources. The average HI/LO signal level relative to the input return is the common mode voltage **Vcm** which, for optimum performance, must not exceed the maximum value indicated in the product specification.

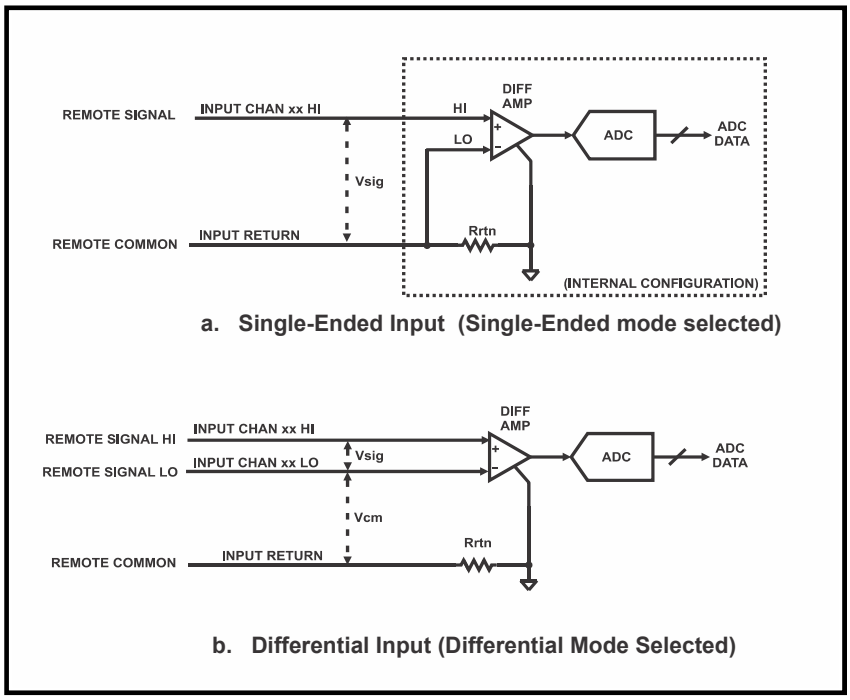

Figure 2.3.1. Input Configurations

2.3.2 Single-Ended Inputs

Single-ended signal sources can be accommodated as shown in Figure 2.3.1a, with the signal line connected to INPUT CHAN xx HI, and the associated INPUT CHAN xx LO input connected to INPUT RETURN at the source. The single-ended operating connection provides suitable performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

CAUTION: If a significant potential difference exists between the remote signal return and INPUT RETURN, a low impedance between the two returns can cause excessive current to flow, which in turn can cause erroneous measurements or possible damage to the board. Return-current should be controlled to less than a few milliamps for best performance, and to less than 100 milliamps to avoid damage.

2.4 Multichannel Input Sync

Analog input converters on the board can be triggered in single-scan bursts from an external source. When configured for input bursts, and with INPUT TRIGGER READY, a HIGH to LOW transition on the TTL INPUT TRIGGER line will acquire a single sample of all active channels.

2.5 Analog Outputs

The four analog output channels are single-ended and have a common signal return, referred to in Table 2.2.1 as OUTPUT RETURN. In general, single-ended outputs should drive only loads that are isolated from system ground. The best results are obtained when the loads also are isolated from each other. The outputs can be disconnected from the system I/O connector under software control, without losing the data values in the output DACs. When disconnected, each output appears as approximately 20-30 KOhms to OUTPUT RETURN.

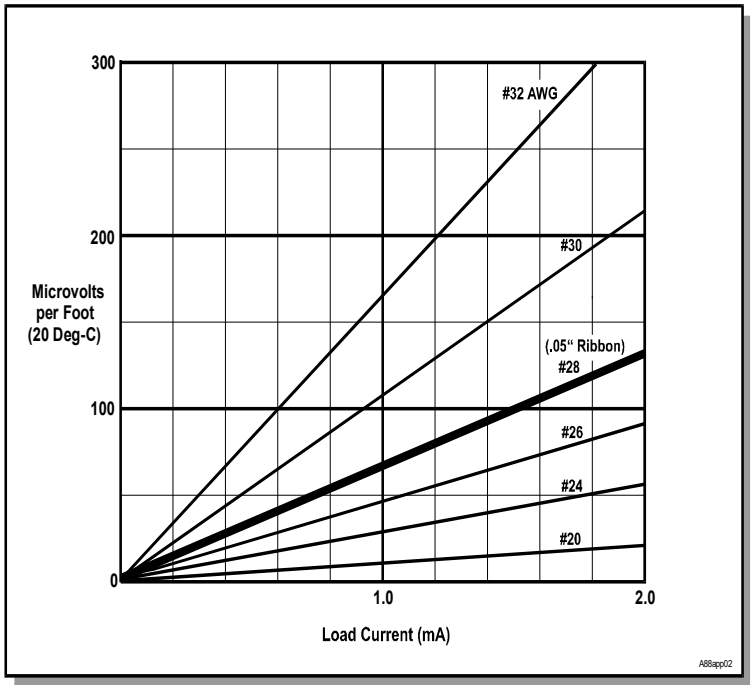

Figure 2.5.1 Voltage Drop in Exterior Cables

The voltage drop in a ribbon cable can be a significant source of error in 16-bit systems, even with relatively short cables driving low-current loads. Figure 2.5.1 shows the effect of load current on the voltage drop in copper wire of various sizes. A 2.0 milliamp load for example, will insert a voltage drop of approximately 130 microvolts *per foot* in conventional #28 AWG ribbon cable; twice that if the return line is equivalent. Several feet of ribbon cable therefore can produce significant errors in even a moderately loaded 16-bit system, in which 1 LSB may represent only 305 microvolts (±10 Volt range). High impedance loads generally will not produce significant DC line loss errors.

2.6 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference calibration. The optimum calibration interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and input signal levels, should be evaluated before troubleshooting of the board itself is attempted. If surface-mount repair capability is not available, a board that is suspected to be defective should be returned to the factory for problem analysis and repair.

2.6.1 Reference Verification

All input and output channels are software-calibrated to an internal voltage reference (Vrange) by an embedded autocalibration software utility. The procedure presented here describes the adjustment of the reference. For applications in which the system must not be powered down, the adjustment can be performed under normal operating conditions while the board is installed on the host.

To eliminate the requirement for a special test connector, the two test points required for reference adjustment, RANGE VREF and VREF RETURN, can be made available at a system breakout connector or test panel. This arrangement also eliminates the necessity of disconnecting the system input/output cable for reference adjustment.

2.6.1.1 Equipment Required

Table 2.6.1 lists the minimum equipment requirements for adjusting the PMC66-24DSI6LN4AO reference. Alternative equivalent equipment may be used.

Table 2.6.1. Reference Verification Equipment

Equipment Description	Manufacturer	Model
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±2.5 Volts to ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Standard 68-Pin, 0.05", subminiature "D" connector, with test leads.	AMP	749621-7

2.6.1.2 Adjustment Procedure

This procedure describes the single adjustment that is necessary to ensure conformance to the product specification.

Adjustment of the internal reference (Vrange) can be performed locally with an internal trimpot, or remotely with a potentiometer connected to the Front Panel System I/O connector if practical, the internal reference trimpot should be used to perform the Vrange adjustment. The adjustment trimpot is accessible from the side of the board as shown in Figure 1.1. Any adjustment seal present on the trimmer should be removed before beginning the procedure, and the trimmer should then be resealed with a suitable sealing agent after the adjustment has been completed.

If the internal Vrange trimmer is inaccessible, adjustment of the reference can be performed remotely by connecting a 20 KOhm potentiometer to the system I/O connector,, as shown in Figure 2.6.2.1. The potentiometer must remain connected after the adjustment procedure has been completed.

This procedure assumes that the board to be adjusted is installed on a host board, and that the host is installed in an operating system. The board can be in any operating mode when the adjustment is performed.

1. Connect the digital multimeter between the PFS_REF Pin-2 (+) and REF_RTN Pin-1 (-) in the Reference Test connector J4 on the PCB.

   Alternatively; Connect the digital multimeter between the RANGE VREF (+) and VREF RETURN (-) pins in the system I/O connector. Refer to Table 2.2.1 for pin assignments.

2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding.

3. Adjust the REFERENCE ADJUSTMENT trimmer until the digital multimeter indication is as indicated here for the installed voltage range

   ±10Volt range: +10.0000 ±0.0015 VDC.
   ±5Volt Range: +5.00000 ±0.0012 VDC.
   ±2.5Volt Range: +2.50000 ±0.0009 VDC.

4. Reference adjustment is complete. Remove all test connections.

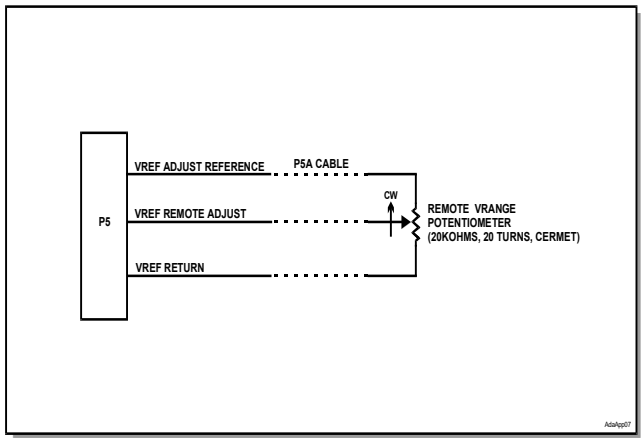

Figure 2.6.2.1. Remote Reference Adjustment

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-24DSI6LN4AO is controlled by a PLX™ PCI-9056 Bus adapter, which is compatible with PCI Specification 2.3, using 66 MHZ or 33 MHz bus and D32 read/write transactions.. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1. All data transfers are long-word D32. Reserved bits in each register are ignored during write operations, and are forced LOW during read operations. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written as LOW.

Table 3.1. Control and Data Registers

Local Addr [1]	Access Mode	Register	Default	Description	Ref
00	R/W	Board Control (BCR)	0095 0823h	Board Control Register (BCR)	3-2
04	R/W	Digital I/O Port	00XX_XXXXh	Digital Port control	3-7
08	R/W	Output Channel 0	0000 8000h	DAC Channel-0 data register.	3.12
0C	R/W	Output Channel 1	0000 8000h	DAC Channel-1 data register.	
10	R/W	Output Channel 2	0000 8000h	DAC Channel-2 data register.	
14	R/W	Output Channel 3	0000 8000h	DAC Channel-3 data register.	
18	RO (DMA)	Input Data Buffer	0XXX XXXXh	Input Data and channel tag	3.5
1C	R/W	Rate Assignment	0040 0032h	Input Rate Assignment.	3.6.1.5
20	R/W	Rate Divisor	0000 0005h	Input Sample rate divisor.	3.6.1.4
24	R/W	AI Buffer Control	0003 FFFEh [2]	Input buffer control and status	3.5.3
28	RO	Buffer Size	0000 0000h	Number of samples in the buffer.	3.5.4
2C	RO	(Reserved)	0000 0000h	---	---
30	RO	(Reserved)	0000 0000h	---	---
34	RO	Board Configuration	00XX XXXXh	Installed firmware and hardware options.	3.10
38	R/W	AO Rate Divisor	0000 0BB8h	24-bit Divisor for the AO rate generator..	3.12.3
3C-7C	--	(Reserved)	0000 0000h	---	---

[1] HEX Offsets from the "PCI base address for local addressing.
[2] 0203 FFFEh if the buffer is read during register default test.

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and analog input range, and consists of 32 control bits and status flags. Table 3.2 provides a brief description of each bit field in the BCR, as well as indicating an associated section in the text.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0095 0823h**

Data Bit	Mode	Designation	Default	Description	Section
D00	R/W	DIFFERENTIAL INPUTS	1	Selects Differential input mode if HIGH, or Single-Ended mode if LOW. Defaults HIGH.	3.6.1.2
D01	R/W	CONTINUOUS SAMPLING	1	Selects the Burst input sampling mode if LOW, or Continuous Sampling mode if HIGH.	3.6.1.3
D2-D4	R/W	(Reserved)	0	---	---
D05	R/W	OFFSET BINARY	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D06	R/W	(Reserved)	0	---	---
D07	R/W	SOFTWARE SYNC *	0	Initiates a local ADC Sync operation when asserted HIGH.	3.6.2
D8-D10	R/W	INTERRUPT A[2..0]	00h	Interrupt event selection. Default is zero.	3.8
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12-D15	R/W	(Reserved)	0	---	---
D16-D18	R/W	LAST[2..0]	05h	Establishes the channel number of the highest active input channel. Defaults to a value of 5 (6 channels).	3.6.1.1
D19	R/W	(Reserved)	0	---	---
D20	RO	INPUTS READY	1	LOW during any change in channel parameters. Asserted HIGH when ADC clocks are stabilized.	3.4.1
D21	R/W	INPUT TRIGGER *	0	When INPUTS READY is HIGH, 'acquires a single value from each active input channel. Clears automatically.	3.6.1.3
D22	R/W	INPUT DC COUPLING	0	Configures analog inputs as DC Coupled when HIGH. (Not recommended)	3.6.4
D23	RO	BUFFER EMPTY	1	Indicates an Empty buffer when HIGH.	3.5.5
D24	RO	BUFFER FULL	0	Indicates a full buffer when HIGH.	3.5.5
D25	RO	BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.5.3.1
D26	R/W	EXTERNAL AO CLOCKING	0	Selects external clocking for the analog outputs. Disables the internal ao rate generator.	3.12.2
D27	RO	OUTPUT STRB READY	0	Indicates that an output strobe will be accepted.	3.12.1
D28	R/W	OUTPUT STROBE *	0	When SIMULTANEOUS OUTPUTS is HIGH, Clocks all output channels to update their respective DAC inputs. Clears automatically.	
D29	R/W	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs strobe simultaneously. When LOW, the outputs are self-clocking..	
D30	R/W	CONNECT OUTPUTS	0	When HIGH, connects the analog outputs to the I/O connector. When LOW, disconnects the outputs.	3.12.2
D31	R/W	INITIALIZE *	0	Initializes board when asserted HIGH. All register defaults are invoked.	3.3

* Clears automatically.

3.3 Configuration and Initialization

3.3.1 Configuration

Configuration is initiated by a PCI bus RESET, and should be required only once after the initial application of power. During board configuration, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	5 seconds

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of 5 seconds, and establishes the following conditions:

- Synchronous Scanning is selected (3.6.1.5),
- The input rate generator is adjusted to 25.6 MHz (3.6.2),
- Analog inputs are AC-coupled. (3.6.4.),
- Analog input sample rate is 10 KSPS (3.6.1.4);
- The analog output rate generator is set to 10 kHz, and is inactive (3.12.3);
- The analog input buffer is reset to empty and is disabled. (3.5),
- The threshold is set to 0003 FFFEh (3.5.3.1),
- All control registers are initialized; all defaults are invoked (3.3.2),
- Digital I/O lines are configured as inputs (3.7),.
- The local interrupt request is asserted by an initialization-completed event (3.3.2,3.).

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

The analog inputs are configured as six differential HI/LO signal pairs or as six single-ended inputs, by the DIFFERENTIAL INPUTS control bit in the BCR. This bit defaults HIGH, selecting the differential configuration. Single-Ended inputs are selected by clearing this control bit LOW. The fullscale input voltage range is determined by an ordering option as either ±10V, ±5V or ±2.5V. The installed range is listed in the BOARD Configuration Table (3.10).

3.4.1 Settling Delays and the INPUTS READY Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the INPUTS READY status flag in the BCR goes LOW during the delay. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "inputs ready" event (Section 3.8.1). The INPUTS READY flag goes low during the following operations for the approximate intervals indicated:

5 Seconds:	Board initialization,
1 us:	Buffer reset, if not in synchronous-scanning mode,
10 us-5 ms:	Buffer reset, if in synchronous-scanning mode,
500 ms:	Sample rate change,
1-500 ms:	ADC synchronization.

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO data buffer, which has a capacity of 256K data values. Data accumulates in the buffer until extracted by the PCI bus from a single register location, indicated as INPUT DATA BUFFER in Table 3.1. Reading an empty buffer returns an indeterminate value.

3.5.2 Data Organization

Each value in the data buffer consists of a 2-bit channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the buffer control register (Table 3.5.3), and the width of the zero-pad field is adjusted accordingly. The zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0018h **Default: 0XXX XXXXh**

Selected Data Width	(Reserved, Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..26]	D[25..24]	D[23..16]	D[15..0]
18 Bits	D[31..26]	D[25..24]	D[23..18]	D[17..0]
20 Bits	D[31..26]	D[25..24]	D[23..20]	D[19..0]
24 Bits	D[31..26]	D[25..24]	---	D[23..0]

3.5.2.1 Channel Tags

If the input channels are not scan-synchronized (Paragraph 3.6.2), the order in which channel data accumulates in the buffer is not generally predictable. For this reason, a channel tag that identifies each input channel is attached to the associated data values in the buffer.

3.5.2.2 Input Data Format

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +5.000 Volts for the ±5V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V range).

3.5.3 Buffer Control Register

The buffer control register (Table 3.5.3) contains the threshold value for the buffer status flag, and also provides controls for clearing the buffer and for disabling the buffer input.

The buffer will ignore input data unless the ENABLER BUFFER INPUT control bit D18 is HIGH, (and if the INPUTS READY status flag in the BCR also is HIGH). To initiate data acquisition, set this bit HIGH. To terminate acquisition, clear the bit LOW.

Table 3.5.3. Buffer Control Register

Offset: 0000 0024h **Default: 0003 FFFEh [3]**

Bit Field	Mode	Designation	Default	Function
D00-D17	R/W	BUFFER THRESHOLD	3 FFFEh	Buffer Threshold Flag.
D18	R/W	ENABLE BUFFER INPUT	0	Enables inputs to the data buffer.
D19	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer
D20-D21	R/W	DATA WIDTH	0	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D22-D23	RO	(Reserved)	---	---
D24	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D25	R/W	BUFFER UNDERFLOW [2,3]	0	Reports buffer underflow (Read on empty)
D26-D31	RO	(Reserved)	---	

[1] Clears automatically. [2] Clear by writing LOW, or by reset.
[3] D25 goes HIGH if buffer is read during a register default test.

NOTE: Since delta-sigma ADC's perform conversions continuously, the initiation and termination of acquisition sequences is controlled by the buffer's 'Clear' and 'Enable' controls.

3.5.3.1 Threshold Status Flag

The amount of data contained in the input buffer controls the BUFFER THRESHOLD FLAG status bit in the BCR, which can be selected also as an interrupt request event. The threshold value can be any value from 1 to FFFF FFFFh. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer control register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

3.5.3.2 Buffer Clearing and Disabling

Asserting the CLEAR BUFFER control bit in the buffer control register resets (empties) the buffer, and holds the buffer in reset for approximately 10 microseconds to allow the internal data pipeline to empty. This bit clears automatically.

Clearing the ENABLE BUFFER INPUT control bit disables inputs to the buffer from the ADC input channels, and halts the accumulation of further input data. Input data already present in the buffer when this bit was asserted remains in the buffer.

3.5.4 Buffer Size Register

This 19-Bit read-only register contains the number of analog input values currently stored in the input data buffer.

Table 3.5.4. Buffer Size Register

Offset: 0000 0028h **Default: 000X XXXXh**

Bit Field	Mode	Buffer Size
D00-D18	RO	Number of samples in buffer
D19-D31	RO	(Reserved)

3.5.5 Buffer Underflow and Overflow Flags

BUFFER OVERFLOW and BUFFER UNDERFLOW status bits in the buffer control register report overflow (write on full) or underflow (read on empty) events. Once set, these status bits remain HIGH until cleared by writing LOW directly, or by an initialization.

3.6 Input Sampling Control

The local controller establishes the following input sampling parameters:

a. Acquisition Mode,
b. Sample clock Generation,
c. Rate Generator Control,
d. Active input channels and input Clocking mode.

NOTE: The digital filter in each ADC requires approximately 100K sample intervals to settle completely to 24 bits, which for example corresponds to 5 seconds at 20KSPS, although 20K intervals or less should provide adequate settling for most applications at the 16-bit level:

The amount of delay actually used after the buffer is enabled is determined by the application software. Five seconds are provided automatically after initialization

3.6.1 Acquisition Mode

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles. To ensure that all converters can be synchronized, all active analog input channels are clocked continuously by the same internal (Input) rate generator.

3.6.1.1 Active Input Channels

The number of active channels is selected by the Bit-Field LAST[2..0] in the BCR, which specifies the last (highest) channel number acquired in a scan.

3.6.1.2 Differential and Single-Ended Operation

Operation is established as ***differentia****l* if the DIFFERENTIAL INPUTS control bit is HIGH in the BCR, or as ***Single-Ended*** if the bit is LOW.

3.6.1.3 Continuous and Burst Mode Sampling

Input acquisition is selected by setting the CONTINUOUS SAMPLING control bit HIGH in the BCR. In this mode all inputs are sampled at the rate of the input rate generator (3,6.1.5). Continuous acquisition can be stopped by clearing the buffer and holding it in reset, or by selecting the burst mode. In the continuous mode, all ADC data is acquired and stored in the buffer.

Triggered BURST MODE sampling is selected by clearing the CONTINUOUS SAMPLING control bit LOW in the BCR. All active channels are sampled once during a burst. A burst is initiated by a burst trigger, and s a simultaneous sampling of all active channels.

A **'Software' Trigger** is generated by setting the INPUT TRIGGER control bit High in the BCR. This bit clears automatically.

A **'Hardware' Trigger** can be acquired **through** the system I/O connector by clearing the INPUT TRIGGER input LOW while the INPUT TRIGGER READY line is HIGH. This input is edge-detected.

3.6.1.4 Sample Clock Generation

The ADC sample rate **Fsamp** is determined by the rate generator frequency **Fgen** and a rate **DIVISOR** as: (all values in decimal).

Fsamp = Fgen / (512 * DIVISOR) , **(3-1)**

where **Fsamp** and **Fgen** are in kilohertz, and **DIVISOR** is defined as:

If Ndiv > 0, then DIVISOR = Ndiv,
If Ndiv = 0, then DIVISOR = 0.5 ,

where **Ndiv** can have any integer value from zero through 25, and **Fgen** has a range of 25.6 MHz through 51.2 MHz. **Fgen** is the frequency of the rate generator.

The Rate divisor integer **DIVISOR** (Table 3.6.1.3-1) is a ***divisor*** for the rate generator.

Table 3.6.1.3-1. Input Rate Divisor Register

Offset: 0000 0020h **Default: 0000 0005h**

Bit Field	Rate Divisor
D[05..00]	RATE DIVISOR (**Ndiv**): 0 - 25
D[31..06]	(Reserved)

Note: The ADC's operate with one of three different oversampling factors (OSF), with each OSF determined by the assigned sample rate, as shown in Table 3.6.1.3-2 for reference. In addition to establishing the sample rate division factor DIVISOR, the integer Ndiv also controls the ADC clocking mode.

Table 3.6.1.3-2. Oversampling Factor (For reference)

Sample Rate Fsamp (KSPS)	Oversampling Factor (OSF)	Divisor Integer Ndiv
2-50	256 * Fsamp	**2 thru 25**
50-100	128 * Fsamp	**1**
100-200	64 * Fsamp	**0**

3.6.1.5 Input Rate Generator Control

Fgen is generated by an internal phase-locked loop (PLL) oscillator. The frequency **Fgen** of the oscillator is related to a reference frequency **Fref** by integers **Nvco** and **Nref** (Table 3.6.1.4-1) as:

$$\mathbf{Fgen} = \mathbf{Fref} * \frac{\mathbf{Nvco}}{\mathbf{Nref}} , \qquad \textbf{(3-2)}$$

where **Nvco** and **Nref** each has a maximum range from 30 to 1000, and **Fref** is the frequency of the reference oscillator, which has a standard frequency of **32.768MHz**. Table 3.6.1.4-3 is a summary of sample rate control parameters.

NOTE: Nvco and Nref each has a maximum range from 30 to 1000. For optimum performance, select the *lowest* possible values for Nvco and Nref, preferably less than 100.

Combining Equation 3-1 and 3-2 produces (3-3) that defines the ratio of **Nvco** and **Nref** required to establish the desired sample rate **Fsamp, once Fref** and **DIVISOR** are determined:

$$\frac{\mathbf{Nvco}}{\mathbf{Nref}} = \frac{\mathbf{Fsamp} * 512 * \mathbf{DIVISOR}}{\mathbf{Fref}\ (32.768\text{MHz})} , \qquad \textbf{(3-3)}$$

where **Nvco** and **Nref** are controlled through the PLL Rate Control register.

Table 3.6.1.5-1. PLL Rate Control Register

Offset: 0000 001Ch **Default: 0040 0032h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D00-D09	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 30-1000.
D10-D15	R/W	(Reserved)	---
D16-D25	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 30-1000.
D26-D31	R/W	(Reserved)	---

* Rate generator defaults to 25.6MHz.

Table 3.6.1.5-2. Summary of PLL Sample Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Factor	**Nvco**	30-1000
Reference Factor	**Nref**	30-1000
Rate Divisor	**Ndiv**	0 - 25
Reference Frequency	**Fref**	Standard value = 32.768MHz

The following example illustrates one of several methods for determining **Nvco** and **Nref**: Calculating the optimum values for integers **Nvco** and **Nref** can often be simplified by converting all variables, including **Fref**, into products of their prime factors):

EXAMPLE: Required sample rate **Fsamp** is **15.360 kHz**. **Fref = 32.768 MHz**:

1. Insert the **Fref** and required **Fsamp** values into Equation 3-3, expressing both in Hertz.

$$\frac{\text{Nvco}}{\text{Nref}} = \frac{15360 * 512 * \text{DIVISOR}}{32768000} .$$

2. Convert **Fref** and **Fsamp** into their prime factors, and simplify the fraction by canceling all factors that are duplicated in the numerator and denominator

$$\frac{\text{Nvco}}{\text{Nref}} = \frac{(2^{10} * 3 * 5) * (2^{9}) * \text{DIVISOR}}{2^{18} * 5^{3}} = \frac{6 * \text{DIVISOR}}{25} .$$

3. Select a value for **DIVISOR** that adjusts the value of the fraction to **between 0.78 and 1.56** (25.6MHz to 51.2MHz /32.768MHz), with unity being ideal. In this case, use **DIVISOR = 4:**

$$\frac{\text{Nvco}}{\text{Nref}} = \frac{24}{25} .$$

4. Multiply both numerator and denominator by an integer that produces the lowest possible in-range values for **Nvco** and **Nref**, which must be **30 or greate**r. In this case, multiply by 2:

$$\frac{\text{Nvco}}{\text{Nref}} = \frac{48}{50} .$$

5. To confirm the results, first use Equation 3-2 to verify that the rate generator frequency **Fgen is within the specified range of 25.6 - 51.2 MHz.** If **Fgen** is out of range, select another **DIVISOR** value in Step-3:

Nvco = 48; Nref = 50.

$$\text{Fgen} = \text{Fref} * \frac{\text{Nvco}}{\text{Nref}}$$

$$= 32{,}768{,}000 \text{ Hz} * \frac{48}{50} = \underline{31{,}457{,}280 \text{ Hz}}. .$$

Finally, use Equation 3-1 to verify the sample rate **Fsamp**:

$$\text{Fsamp} = \frac{\text{Fgen}}{512 * \text{DIVISOR}}$$

$$= \frac{31{,}457{,}280 \text{ Hz}}{512 * 4} = \underline{15{,}360 \text{ KHz}} .$$

3.6.2 Channel Synchronization

Clocking multiple converters from a single sample clock prevents the *sampling drift* that occurs when converters are clocked from different sources. Adding *Synchronization* causes the converters in all channels to initiate conversions simultaneously and in phase.

All channels are synchronized automatically after initialization or after a change in the sampling clock setup. To invoke synchronization at any time, set the SOFTWARE SYNC control bit HIGH in the BCR. The INPUTS READY flag in the BCR is LOW during synchronization, and is available as in interrupt event as listed in Table 3.8.1.

3.6.3 Multiboard Operation

Multiple PMC66-24DSI6LN4AO boards can be connected together to share a common burst triggering of analog inputs or external strobing of the analog outputs.

3.6.4 Input Coupling

All analog input channels are AC coupled by default. The low-end of the AC-coupled passband is -3dB at:

-3dB Low-end Frequency (Hz) = Fsamp (Hz)/ 48,000.

The inputs can be configured to be ***DC coupled*** by setting the INPUT DC COUPLING control bit HIGH in the BCR. However, this is a diagnostic mode with increased noise levels, and is not recommended for general operation.

3.7 DIGITAL IO PORT

The digital port is controlled by the Digital I/O Port register, and provides 8 bits of bidirectional input/output digital data, as well as a dedicated output control bit and a dedicated input status bit, as shown in Table 3.7.1. The IO DATA DIRECTION control bit establishes the direction of the eight bidirectional data bits, which are configured as outputs if the control bit is HIGH or as inputs if the control bit is LOW. The dedicated input and output control bits are not affected by the direction control bit. An external HIGH hardware logic level is associated with a HIGH value ("1") in the Digital I/O Port register [D10, D8..0] bit field.

Functions of all bits in this port are determined entirely by specific system requirements.

Table 3.7.1. Digital I/O Port Register

Offset: 0004h **Default: 0000 0XXXh**

Bit	Mode	Designation	Def	Description
D00	R/W	IO DATA 00	X	Bidirectional digital I/O lines
D01	R/W	IO DATA 01	X	
D02	R/W	IO DATA 02	X	
D03	R/W	IO DATA 03	X	
D04	R/W	IO DATA 04	X	
D05	R/W	IO DATA 05	X	
D06	R/W	IO DATA 06	X	
D07	R/W	IO DATA 07	X	
D08	RO	IO CONTROL INPUT	X	I/O port dedicated input line
D09	R/W	IO CONTROL OUTPUT	0	I/O port dedicated output line
D10	R/W	IO DATA DIRECTION	0	HIGH => I/O DATA XX lines are outputs LOW => I/O DATA XX lines are inputs
D11-D31	---	(Reserved)	---	Inactive

3.8 Interrupt Control

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1. Interrupt Event Selection

Interrupt [2..0]	Interrupt Event
0	Initialization completed. Default state.
1	Inputs_Ready flag LOW-to-HIGH transition
2	Analog input buffer threshold flag, LOW-to-HIGH transition
3	Analog input buffer threshold flag, HIGH-to-LOW transition
4	Analog input buffer overflow or underflow flag asserted
5	(Reserved)
6	(Reserved)
7	Output Strobe acknowledged

3.9 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master. Refer to the PEX8311 reference manual for a description of DMA configuration registers.

3.9.1 Block Mode

Table 3.9.1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For most applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.9.1. Typical DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.9.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.9.2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.9.2. Typical DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The Bus adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group is retained until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the bus adapter to the PCI bus, and no samples are lost.

3.10 Board Configuration Register

The read-only board configuration register (Table 3.10.1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.10.1. Board Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

Bit field	Description
D00-D15	Firmware Revision
D16	HIGH if 6 Input channels are available, Low if 4 are available.
D17	HIGH if 4 Output channels are available
D18-D19	Indicates Input Voltage Range: 0 => ±10V 1 => ±5V 2 => ±2.5V 3 => (Reserved)
D20	Indicates Image Filter frequency: 0 => 270kHz (Standard) 1 => Custom Frequency.
D21	HIGH for extended temperature operation, LOW for commercial.
D22-D31	(Reserved)

3.11 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance is suspended. Abrupt changes include:

- A change in sample rate,
- Major step-change,
- System or local reset, or power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

3.12 Analog Output Channels

Writing a 16-bit value to any of the four analog Output Channel registers listed in Table 3-1 initiates a transfer of the output value to the corresponding analog output channel. The output registers are configured as shown in Table 3.12.1, and the output value can be formatted in either offset binary or in two's complement, as selected by the OFFSET BINARY control bit in the BCR.

Table 3.12.1. Analog Output Data Register

Reg Bit	Mode	Description
D00	R/W	Least significant Bit (LSB)
D01-D14	R/W	Intermediate Bits
D15	R/W	Most Significant bit (MSB)
D16-D31	---	Inactive

NOTE: The output disconnect switches (3.12.3) default to 'open' (not connected). To obtain an output at the System I/O connector, the CONNECT OUTPUTS control bit *must* be HIGH in the BCR.

3.12.1 Output Clocking (Strobing)

The analog outputs can be clocked (strobed) from any of the four sources listed in Table 3.12.2.

Table 3.12.2. Analog Output Clock Sources

Clock Source	Description *	Clocking Mode
Internal ao_rate generator (3.12.3)	Fmclk/Nrate_ao,2Hz to Fao-max	Simultaneous
External clock, falling edge	Output strobe, Zero to Fao-max	
Software clock	BCR D28, Zero to Fao-max	
Automatically	Self-clocking, Zero to Fao-max	Sequential

* Fao_max = maximum output clocking frequency.

SIMULTANEOUS CLOCKING:

When operating in the **Simultaneous Clocking** mode, the output values are transferred serially from the data registers to output holding registers, and all are clocked simultaneously when a clock occurs. Only revised values experience a change at the outputs.

Simultaneous clocking is selected by setting the SIMULTANEOUS OUTPUTS control bits HIGH in the BCR. If the EXT OUTPUT CLOCKING control bit also is HIGH, the outputs are clocked by a falling edge of the *external clock input* at the System I/O connector.

If EXT OUTPUT CLOCKING is LOW, then the external clock is ignored, and the clocking rate is controlled by the ***AO Rate generator*** (Section 3.12.3).

A **Software clock** can be generated at any time in Simultaneous mode by setting the OUTPUT STROBE control bit HIGH in the BCR. This bit clears automatically.

NOTE: In order for a strobe to be acknowledged, the OUTPUT STROBE READY flag in the BCR must be HIGH.

SEQUENTIAL CLOCKING:

If SIMULTANEOUS OUTPUTS is LOW in the BCR, **Sequential clocking** is selected, and the outputs become self-clocking. Each channel is automatically clocked immediately at the end of the output data serial transfer.

3.12.2 Analog Outputs Rate Generator

The internal analog output rate generator provides an output clock **Fclk_ao** controlled by the 24-bit NRATE AO control field in the AO Rate Generator Divisor register (Table 3.12-3). The rate generator is active when SIMULTANEOUS OUTPUTS is HIGH in the BCR and EXTERNAL CLOCKING is LOW.

Table 3.12.3. AO Rate Generator Divisor

Offset: 0038h **Default: 0000_0BB8h**

Data Bit	Mode	Designation	Description
D00-D23	R/W	NRATE AO	AO Rate Generator divisor.
D24-D31	RO	(Reserved)	Inactive. Returns all-zero.

The output clocking rate **Fclk_ao** is calculated by the formula:

Fclk_ao = Fmclk / NRATE_AO ,

where Fmclk is the frequency of the board's master clock frequency, standard at **30.000 MHz**, and **NRATE_AO is the divisor specified by the AO Rate Generator Divisor register.** Clocking rates above **252 kHz** can produce unpredictable results and are not recommended.

Example: { Fmclk=30MHz, NRATE_AO = 3000 (0BB8h) } => Fclk_ao = 10.000 kHz.

3.12.3 Analog Outputs Disconnect

The analog outputs are connected to the system I/O connector when the CONNECT OUTPUTS control bit is asserted HIGH. For applications in which driven devices must not be exposed to the voltage excursions present at the analog outputs during selftest operations, the analog outputs can be disconnected from the system I/O connector by clearing the CONNECT OUTPUTS control bit LOW in the BCR. The analog outputs default to the disabled state (control bit LOW) after initialization.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PMC66-24DSI6LN4AO board contains three dual delta-sigma 24-Bit A/D converters and all supporting functions necessary for adding analog I/O capability to a PCIe104 stack. A PCI Express interface adapter (Figure 4.1) provides the interface between the controlling bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions.

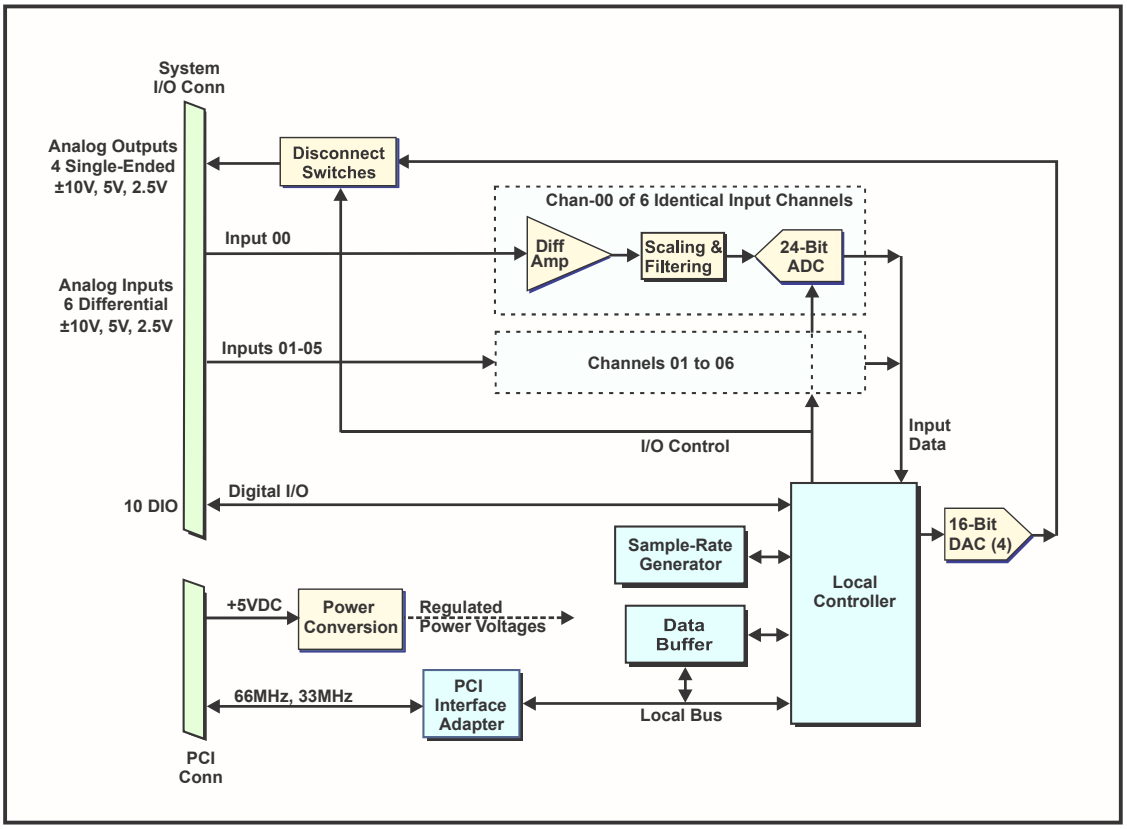

Figure 4.1. Functional Block Diagram

4.2 Analog Inputs

The six analog inputs (Figure 4.1) acquire input signals through a dedicated ADC in each channel. Analog-to-digital conversions are performed upon only external inputs at the system I/O connector. Common mode interference is rejected by a differential amplifier when the inputs are configured for differential operation.

A scaling and filtering network adjusts the maximum level of the input signal to the full-scale input range of 2.0 VRMS required by the ADC, and provides a 2-Pole lowpass i**mage filter** to eliminate high frequency harmonics generated by the ADC's digital filter.

The final conditioned, scaled and filtered input signal is digitized by each ADC into a 24-BIt serial data word that is deserialized into parallel format by the local controller. The local controller then attaches a 3-bit channel tag to the data word.

Antialias filtering is provided by each ADC in the form of a lowpass digital filter with a very sharp cutoff frequency at approximately 40-50 percent of the sampling frequency. The digital filter has no effect at multiples of the sampling clock, and to prevent extraneous signal frequency components within these "filter images" from appearing in the passband, hardware image filters provide lowpass filtering within the digital filter images.

4.3 Sampling Clock

An internal sample rate generator provides a frequency range of 25.6 - 51.2 MHz, which is divided down by software-specified integers to provide sample rates from 2.0 KSPS to 200 KSPS.

4.4 Analog Outputs

Four analog output channels can be clocked either internally with software, or externally by a hardware strobe. The analog outputs have the same voltage range as the analog inputs, and each channel contains a dedicated 16-Bit DAC.

In the continuous clocking mode, each channel value is routed immediately to the associated DAC, In the simultaneous mode, channel is held in an intermediate register until a strobe transfers the data immediately to the channel output.

4.5 Digital I/O

A Digital I/O port provides eight bidirectional pins, plus one uncommitted input and one uncommitted output. All pins are connected internally to +VDC through 33K, and are compatible with TTL and LVTTL logic levels.

4.6 Power Control

Regulated precision supply voltages of +5 and ±14 Volts are required by the internal analog networks. Multiple DC/DC converters in the power conditioner use the coarsely regulated +5.0V input power from the PCI bus to produce preregulated DC voltages that subsequently are postregulated with linear regulators to the required supply voltages. Linear regulation ensures that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local control registers in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

Local Addr [1]	Access Mode	Register	Default	Description	Ref
00	R/W	Board Control (BCR)	0095 0823h	Board Control Register (BCR)	3-2
04	R/W	Digital I/O Port	00XX_XXXXh	Digital Port control	3-7
08	R/W	Output Channel 0	0000 8000h	DAC Channel-0 data register.	3.12
0C	R/W	Output Channel 1	0000 8000h	DAC Channel-1 data register.	
10	R/W	Output Channel 2	0000 8000h	DAC Channel-2 data register.	
14	R/W	Output Channel 3	0000 8000h	DAC Channel-3 data register.	
18	RO (DMA)	Input Data Buffer	0XXX XXXXh	Input Data and channel tag	3.5
1C	R/W	Rate Assignment	0040 0032h	Input Rate Assignment.	3.6.1.5
20	R/W	Rate Divisor	0000 0005h	Input Sample rate divisor.	3.6.1.4
24	R/W	AI Buffer Control	0003 FFFEh [2]	Input buffer control and status	3.5.3
28	RO	Buffer Size	0000 0000h	Number of samples in the buffer.	3.5.4
2C	RO	(Reserved)	0000 0000h	---	---
30	RO	(Reserved)	0000 0000h	---	---
34	RO	Board Configuration	00XX XXXXh	Installed firmware and hardware options.	3.10
38	R/W	AO Rate Divisor	0000 0BB8h	24-bit Divisor for the AO rate generator..	3.12.3
3C-7C	--	(Reserved)	0000 0000h	---	---

[1] HEX Offsets from the "PCI base address for local addressing.
[2] 0203 FFFEh if the buffer is read during register default test.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0095 0823h**

Data Bit	Mode	Designation	Default	Description	Section
D00	R/W	DIFFERENTIAL INPUTS	1	Selects Differential input mode if HIGH, or Single-Ended mode if LOW. Defaults HIGH.	3.6.1.2
D01	R/W	CONTINUOUS SAMPLING	1	Selects the Burst input sampling mode if LOW, or Continuous Sampling mode if HIGH.	3.6.1.3
D2-D4	R/W	(Reserved)	0	---	---
D05	R/W	OFFSET BINARY	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D06	R/W	(Reserved)	0	---	---
D07	R/W	SOFTWARE SYNC *	0	Initiates a local ADC Sync operation when asserted HIGH.	3.6.2
D8-D10	R/W	INTERRUPT A[2..0]	00h	Interrupt event selection. Default is zero.	3.8
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12-D15	R/W	(Reserved)	0	---	---
D16-D18	R/W	LAST[2..0]	05h	Establishes the channel number of the highest active input channel. Defaults to a value of 5 (6 channels).	3.6.1.1
D19	R/W	(Reserved)	0	---	---
D20	RO	INPUTS READY	1	LOW during any change in channel parameters. Asserted HIGH when ADC clocks are stabilized.	3.4.1
D21	R/W	INPUT TRIGGER *	0	When INPUTS READY is HIGH, 'acquires a single value from each active input channel. Clears automatically.	3.6.1.3
D22	R/W	INPUT DC COUPLING	0	Configures analog inputs as DC Coupled when HIGH. (Not recommended)	3.6.4
D23	RO	BUFFER EMPTY	1	Indicates an Empty buffer when HIGH.	3.5.5
D24	RO	BUFFER FULL	0	Indicates a full buffer when HIGH.	3.5.5
D25	RO	BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.5.3.1
D26	R/W	EXTERNAL AO CLOCKING	0	Selects external clocking for the analog outputs. Disables the internal ao rate generator.	3.12.2
D27	RO	OUTPUT STRB READY	0	Indicates that an output strobe will be accepted.	3.12.1
D28	R/W	OUTPUT STROBE *	0	When SIMULTANEOUS OUTPUTS is HIGH, Clocks all output channels to update their respective DAC inputs. Clears automatically.	
D29	R/W	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs strobe simultaneously. When LOW, the outputs are self-clocking..	
D30	R/W	CONNECT OUTPUTS	0	When HIGH, connects the analog outputs to the I/O connector. When LOW, disconnects the outputs.	3.12.2
D31	R/W	INITIALIZE *	0	Initializes board when asserted HIGH. All register defaults are invoked.	3.3

* Clears automatically.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0018h **Default: 0XXX XXXXh**

Selected Data Width	(Reserved, Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..26]	D[25..24]	D[23..16]	D[15..0]
18 Bits	D[31..26]	D[25..24]	D[23..18]	D[17..0]
20 Bits	D[31..26]	D[25..24]	D[23..20]	D[19..0]
24 Bits	D[31..26]	D[25..24]	---	D[23..0]

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3. Buffer Control Register

Offset: 0000 0024h **Default: 0003 FFFEh [3]**

Bit Field	Mode	Designation	Default	Function
D00-D17	R/W	BUFFER THRESHOLD	3 FFFEh	Buffer Threshold Flag.
D18	R/W	ENABLE BUFFER INPUT	0	Enables inputs to the data buffer.
D19	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer
D20-D21	R/W	DATA WIDTH	0	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D22-D23	RO	(Reserved)	---	---
D24	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D25	R/W	BUFFER UNDERFLOW [2,3]	0	Reports buffer underflow (Read on empty)
D26-D31	RO	(Reserved)	---	

[1] Clears automatically. [2] Clear by writing LOW, or by reset.
[3] D25 goes HIGH if the buffer is read during a0 register default test.

Table 3.5.4. Buffer Size Register

Offset: 0000 0028h **Default: 000X XXXXh**

Bit Field	Mode	Buffer Size
D00-D18	RO	Number of samples in buffer
D19-D31	RO	(Reserved)

Table 3.6.1.3-1. Input Rate Divisor Register

Offset: 0000 0020h **Default: 0000 0005h**

Bit Field	Rate Divisor
D[05..00]	RATE DIVISOR (**Ndiv**): 0 - 25
D[31..06]	(Reserved)

Table 3.6.1.5-1. PLL Rate Control Register

Offset: 0000 001Ch **Default: 0040 0032h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D00-D09	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 30-1000.
D10-D15	R/W	(Reserved)	---
D16-D25	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 30-1000.
D26-D31	R/W	(Reserved)	---

* Rate generator defaults to 25.6MHz.

Table 3.6.1.4-2. Summary of PLL Sample Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Factor	**Nvco**	30-1000
Reference Factor	**Nref**	30-1000
Rate Divisor	**Ndiv**	0 - 25
Reference Frequency	**Fref**	Standard value = 32.768MHz

Table 3.7.1. Digital I/O Port Register

Offset: 0004h **Default: 0000 0XXXh**

Bit	Mode	Designation	Def	Description
D00	R/W	IO DATA 00	X	Bidirectional digital I/O lines
D01	R/W	IO DATA 01	X	
D02	R/W	IO DATA 02	X	
D03	R/W	IO DATA 03	X	
D04	R/W	IO DATA 04	X	
D05	R/W	IO DATA 05	X	
D06	R/W	IO DATA 06	X	
D07	R/W	IO DATA 07	X	
D08	RO	IO CONTROL INPUT	X	I/O port dedicated input line
D09	R/W	IO CONTROL OUTPUT	0	I/O port dedicated output line
D10	R/W	IO DATA DIRECTION	0	HIGH => I/O DATA XX lines are outputs LOW => I/O DATA XX lines are inputs
D11-D31	---	(Reserved)	---	Inactive

Table 3.8.1. Interrupt Event Selection

Interrupt [2..0]	Interrupt Event
0	Initialization completed. Default state.
1	Inputs_Ready flag LOW-to-HIGH transition
2	Analog input buffer threshold flag, LOW-to-HIGH transition
3	Analog input buffer threshold flag, HIGH-to-LOW transition
4	Analog input buffer overflow or underflow flag asserted
5	(Reserved)
6	(Reserved)
7	Output Strobe acknowledged

Table 3.9.1. Typical DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.9.2. Typical DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.10.1. Board Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

Bit field	Description
D00-D15	Firmware Revision
D16	HIGH if 6 Input channels are available, Low if 4 are available.
D17	HIGH if 4 Output channels are available
D18-D19	Indicates Input Voltage Range: 0 => ±10V 1 => ±5V 2 => ±2.5V 3 => (Reserved)
D20	Indicates Image Filter frequency: 0 => 270kHz (Standard) 1 => Custom Frequency.
D21	HIGH for extended temperature operation, LOW for commercial.
D22-D31	(Reserved)

Table 3.12. Analog Output Data Register

Reg Bit	Mode	Description
D00	R/W	Least significant Bit (LSB)
D01-D14	R/W	Intermediate Bits
D15	R/W	Most Significant bit (MSB)
D16-D31	---	Inactive

Table 3.12.2. Analog Output Clock Sources

Clock Source	Description *	Clocking Mode
Internal ao_rate generator (3.12.3)	Fmclk/Nrate_ao,2Hz to Fao-max	Simultaneous
External clock, falling edge	Output strobe, Zero to Fao-max	
Software clock	BCR D28, Zero to Fao-max	
Automatically	Self-clocking, Zero to Fao-max	Sequential

* Fao_max = maximum output clocking frequency.

Table 3.12-3. AO Rate Generator Divisor

Offset: 0038h Default: 0000_0BB8h

Data Bit	Mode	Designation	Description
D00-D23	R/W	NRATE AO	AO Rate Generator divisor.
D24-D31	RO	(Reserved)	Inactive. Returns all-zero.

APPENDIX-B

SOFTWARE MIGRATON from the ADADIO and 24DSI6LN

APPENDIX-B

Software Migration from the ADADIO and 24DSI6LN

PMC66-24DSI6LN4AO software addresses specific sections of ADADIO and 24DSI6LN operation. This appendix describes the more significant migration issues, and is provided as a general guide rather than a definitive list of requirements or changes.

B.1 Introduction

- In general, controls related to analog inputs are similar the control of PCIe104-24DSI6LN analog inputs. This is true also of the Digital IO port.
- Control of the analog outputs is essentially identical to control of the ADADIO analog outputs.
- Due to the AC-coupled nature of the analog inputs, Autocalibration is not implemented. This is true by default for the 24DSI6LN, for which increased precision is not required. High-precision resistors provide the high accuracy required for the analog outputs, and eliminate the calibration DACs used on the ADADIO.

B.2 Control Register Table and the BCR

(Referring to paragraphs in this manual, e.g.: 3.0 - 3.4.1):

3.0: Control and Data Registers;

- Additional control registers support a modified rate generator, an upgraded input buffer and a Board Configuration register.

3.1: Board Control Register (Similar to ADADIO):

- The AIM[], LBC[] and CM[] control fields have been replaced with discrete control bits DIFFERENTIAL INPUTS and CONTINUOUS SAMPLING. The CAL STATUS FLAG bit and has been removed.
- Control field SIZE[] and flag bit AUTOCAL STATUS FLAG have been removed.
- Status flag BUFFER HALF FULL has been replaced by BUFFER THRESHOLD FLAG.
- The CHANNELS READY flag has been renamed as the INPUTS READY flag.
- The ASYNCHRONOUS SCAN control bit has been eliminated, since all active channels are *always* synchronized.

B.3 Analog Inputs:

3.4: Inputs Configuration (ADADIO):

- Differential or Single Ended configuration of the inputs is selected by the DIFFERENTIAL INPUTS control bit in the BCR.

3.5.1 - 3.5.5: Input Data Buffer (24DSI6LN):

- The input buffer is now a 266K-sample FIFO, and all references to the original 32K-sample virtual buffer have been removed.
- Buffer Control bit D18 has been renamed from "Disable Buffer Input to "Enable Buffer Input", thereby preventing the buffer from filling with probably useless data after every initialization. Since the buffer is always empty after initialization, the default register field is less subject to variations.

B.4 Input Sampling Control:

3.6 - 3.6.1.3: Inputs Configuration (ADADIO):

- Active Input channels selection, Differential/Single-Ended operation, Continuous/Burst sampling.

3.6.1.4 - 3.6.1.5: Sample Clock Generation (24DSI6LN):

- Control of the PLL sample rate generator.

3.6.2 - 3.6.4: Sample Clock Generation (24DSI6LN):

- Channel synchronization.

B.5 Digital IO Port: (24DSI6LN):

3.7: (24DSI6LN):

B.6 Interrupts, DMA, Board Configuration (24DSI6LN):

3.8: Interrupts

3.9: DMA (Inputs)

3.10: Board Configuration

3.11: Settling Times

B.7 Analog Output Channels; (ADADIO):

3.12: Analog Output Channels

3.12-1: Output Strobe

3.12-2: Analog Outputs Rate Generator

3.12-3: Analog Outputs Disconnect

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