Serial I/O Cables

Description
And
Connection Diagrams

CABLEx-SIO4B-STD2-DB9x

For the following products:

SIO4B/BX used in differential mode
(ex. RS485, HDLC, raw synchronous, etc)

Preliminary
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PREFACE

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This document provides information on the description and connection diagrams for serial IO cables.

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Introduction

This document includes descriptions and pin-out for serial I/O cables for SIO4B/BX family of boards. These boards have the same high-density SCSI3 type connector so that they can be interchanged in a system without changing the serial I/O cables.

NOTE: Since the SIO4B/BX family of cards can accommodate many different protocols, the pin assignments for the DB9 connectors do not match any unique specification. However, General Standards Corporation can accommodate special pin assignments at the time you place the order. Please contact us for more information.

Cable part numbers for these SIO4B/BX boards are:

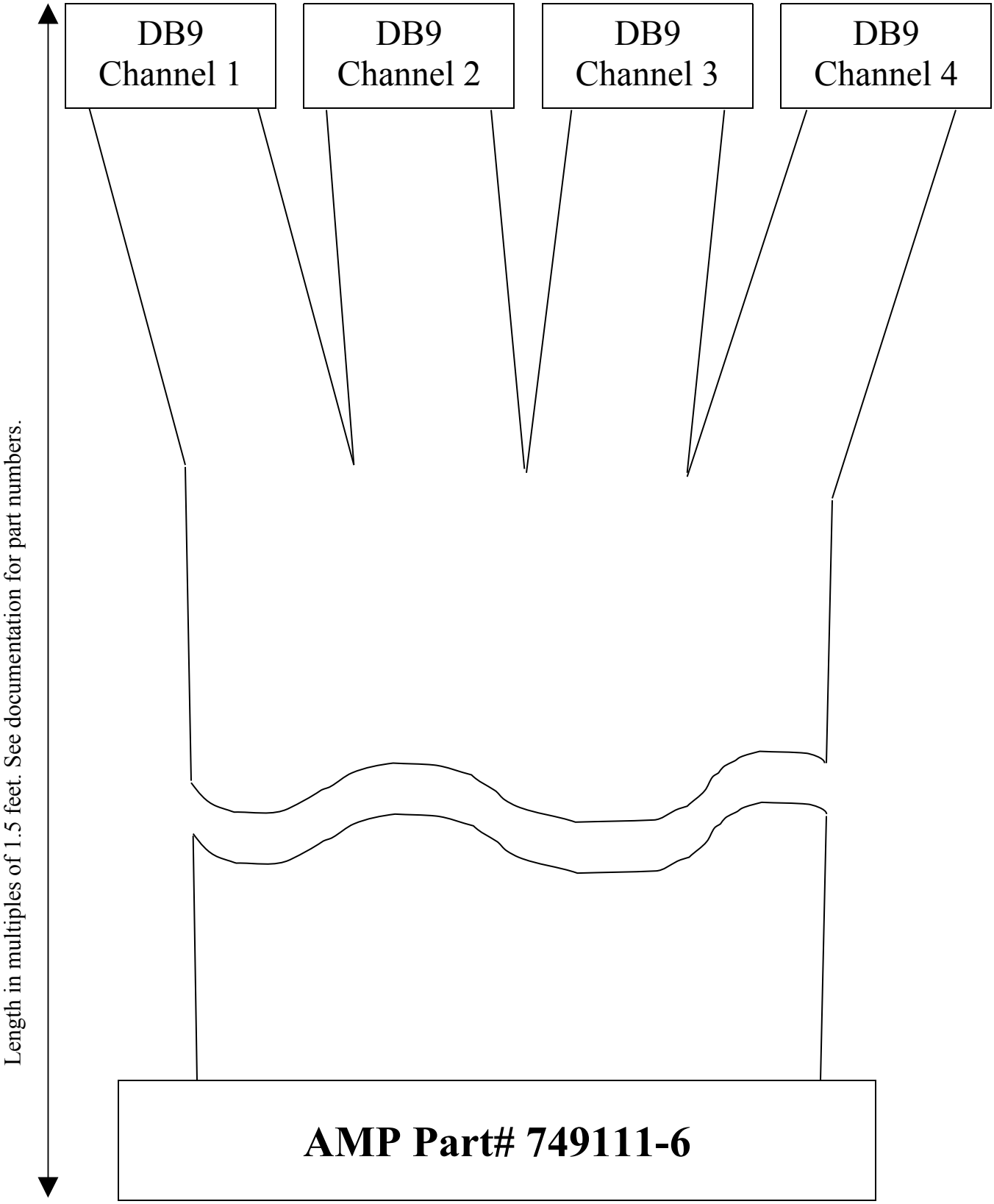
1) **CABLEx-SIO4B-STD2-DB9x**
   - x => length in feet (multiple of 1.5 ft, in lengths up to 100 feet)
   - STD2 => standard wiring v2 diagram per diagram attached
   - DB9x => Four DB9 connectors are attached to the user end of the cable.
     DB9P indicates male connectors (P = pins, male)
     DB9S indicates female connectors (S = sockets, female)

2) **CABLEx-SIO4B-FLAT**
   - x => length in feet (multiple of 1.5 ft, in lengths up to 100 feet)
   - FLAT => designates a 68-pin connector on SIO4BX end only.

These cables use standard 68 conductor 'twist-n-flat' (also known as 'vari-twist') cable. It is made up of twisted pairs with a flat area every 1.5 feet. The conductor spacing in the flat area is standard 50 mil allowing connections to standard IDC connectors.

The pin-out assures that each differential signal is routed to a single twisted pair in the cable. When using single ended protocols, like RS232, only the negative wire is used (TxD-, RxD-, CTS-, etc).

SIO4B/BX card family cable overview:



Cable connections for the SIO4B/BX:							
Board Pin #	**DB9 Pin #**	**DTE Mode Signal:**	**DCE Mode Signal:**	**Board Pin #**	**DB9 Pin #**	**DTE Mode Signal:**	**DCE Mode Signal:**
1		Ch1 AuxC + *		35		Ch3 AuxC + *	
2		Ch1 AuxC - *		36		Ch3 AuxC - *	
3		Ch1 DCD + *		37		Ch3 DCD + *	
4		Ch1 DCD - *		38		Ch3 DCD - *	
5		Ch1 CTS +	Ch1 RTS +	39		Ch3 CTS +	Ch3 RTS +
6		Ch1 CTS -	Ch1 RTS -	40		Ch3 CTS -	Ch3 RTS -
7	3	Ch1 RxD +	Ch1 TxD +	41	3	Ch3 RxD +	Ch3 TxD +
8	8	Ch1 RxD -	Ch1 TxD -	42	8	Ch3 RxD -	Ch3 TxD -
9	4	Ch1 RxC +	Ch1 TxC +	43	4	Ch3 RxC +	Ch3 TxC +
10	9	Ch1 RxC -	Ch1 TxC -	44	9	Ch3 RxC -	Ch3 TxC -
11		Ch1 RTS +	Ch1 CTS +	45		Ch3 RTS +	Ch3 CTS +
12		Ch1 RTS -	Ch1 CTS -	46		Ch3 RTS -	Ch3 CTS -
13	1	Ch1 TxD +	Ch1 RxD +	47	1	Ch3 TxD +	Ch3 RxD +
14	6	Ch1 TxD -	Ch1 RxD -	48	6	Ch3 TxD -	Ch3 RxD -
15	2	Ch1 TxC +	Ch1 RxC +	49	2	Ch3 TxC +	Ch3 RxC +
16	7	Ch1 TxC -	Ch1 RxC -	50	7	Ch3 TxC -	Ch3 RxC -
17	5	Ch 1 GND		51	5	Ch 3 GND	
18	5	Ch 2 GND		52	5	Ch 4 GND	
19		Ch2 CTS +	Ch2 RTS +	53		Ch4 CTS +	Ch4 RTS +
20		Ch2 CTS -	Ch2 RTS -	54		Ch4 CTS -	Ch4 RTS -
21	3	Ch2 RxD +	Ch2 TxD +	55	3	Ch4 RxD +	Ch4 TxD +
22	8	Ch2 RxD -	Ch2 TxD -	56	8	Ch4 RxD -	Ch4 TxD -
23	4	Ch2 RxC +	Ch2 TxC +	57	4	Ch4 RxC +	Ch4 TxC +
24	9	Ch2 RxC -	Ch2 TxC -	58	9	Ch4 RxC -	Ch4 TxC -
25		Ch2 RTS +	Ch2 CTS +	59		Ch4 RTS +	Ch4 CTS +
26		Ch2 RTS -	Ch2 CTS -	60		Ch4 RTS -	Ch4 CTS -
27	1	Ch2 TxD +	Ch2 RxD +	61	1	Ch4 TxD +	Ch4 RxD +
28	6	Ch2 TxD -	Ch2 RxD -	62	6	Ch4 TxD -	Ch4 RxD -
29	2	Ch2 TxC +	Ch2 RxC +	63	2	Ch4 TxC +	Ch4 RxC +
30	7	Ch2 TxC -	Ch2 RxC -	64	7	Ch4 TxC -	Ch4 RxC -
31		Ch2 DCD + *		65		Ch4 DCD + *	
32		Ch2 DCD - *		66		Ch4 DCD - *	
33		Ch2 AuxC + *		67		Ch4 AuxC + *	
34		Ch2 AuxC - *		68		Ch4 AuxC - *	

***** These signals only present on the SIO4BX. They are reserved on the SIO4B.

Cable connections for the SIO4B/BX-SYNC:							
Board Pin #	**DB9 Pin #**	**DTE Mode Signal:**	**DCE Mode Signal:**	**Board Pin #**	**DB9 Pin #**	**DTE Mode Signal:**	**DCE Mode Signal:**
1		Ch1 RxAuxC/TxAuxC + *		35		Ch3 RxAuxC/TxAuxC + *	
2		Ch1 RxAuxC/TxAuxC - *		36		Ch3 RxAuxC/TxAuxC - *	
3		Ch1 RxSp/TxSp + *		37		Ch3 RxSp/TxSp + *	
4		Ch1 RxSp/TxSp - *		38		Ch3 RxSp/TxSp - *	
5		Ch1 RxE +	Ch1 TxE +	39		Ch3 RxE +	Ch3 TxE +
6		Ch1 RxE -	Ch1 TxE -	40		Ch3 RxE -	Ch3 TxE -
7	3	Ch1 RxD +	Ch1 TxD +	41	3	Ch3 RxD +	Ch3 TxD +
8	8	Ch1 RxD -	Ch1 TxD -	42	8	Ch3 RxD -	Ch3 TxD -
9	4	Ch1 RxC +	Ch1 TxC +	43	4	Ch3 RxC +	Ch3 TxC +
10	9	Ch1 RxC -	Ch1 TxC -	44	9	Ch3 RxC -	Ch3 TxC -
11		Ch1 TxE +	Ch1 RxE +	45		Ch3 TxE +	Ch3 RxE +
12		Ch1 TxE -	Ch1 RxE -	46		Ch3 TxE -	Ch3 RxE -
13	1	Ch1 TxD +	Ch1 RxD +	47	1	Ch3 TxD +	Ch3 RxD +
14	6	Ch1 TxD -	Ch1 RxD -	48	6	Ch3 TxD -	Ch3 RxD -
15	2	Ch1 TxC +	Ch1 RxC +	49	2	Ch3 TxC +	Ch3 RxC +
16	7	Ch1 TxC -	Ch1 RxC -	50	7	Ch3 TxC -	Ch3 RxC -
17	5	Ch 1 GND		51	5	Ch 3 GND	
18	5	Ch 2 GND		52	5	Ch 4 GND	
19		Ch2 RxE +	Ch2 TxE +	53		Ch4 RxE +	Ch4 TxE +
20		Ch2 RxE -	Ch2 TxE -	54		Ch4 RxE -	Ch4 TxE -
21	3	Ch2 RxD +	Ch2 TxD +	55	3	Ch4 RxD +	Ch4 TxD +
22	8	Ch2 RxD -	Ch2 TxD -	56	8	Ch4 RxD -	Ch4 TxD -
23	4	Ch2 RxC +	Ch2 TxC +	57	4	Ch4 RxC +	Ch4 TxC +
24	9	Ch2 RxC -	Ch2 TxC -	58	9	Ch4 RxC -	Ch4 TxC -
25		Ch2 TxE +	Ch2 RxE +	59		Ch4 TxE +	Ch4 RxE +
26		Ch2 TxE -	Ch2 RxE -	60		Ch4 TxE -	Ch4 RxE -
27	1	Ch2 TxD +	Ch2 RxD +	61	1	Ch4 TxD +	Ch4 RxD +
28	6	Ch2 TxD -	Ch2 RxD -	62	6	Ch4 TxD -	Ch4 RxD -
29	2	Ch2 TxC +	Ch2 RxC +	63	2	Ch4 TxC +	Ch4 RxC +
30	7	Ch2 TxC -	Ch2 RxC -	64	7	Ch4 TxC -	Ch4 RxC -
31		Ch2 RxAuxC/TxAuxC + *		65		Ch4 RxAuxC/TxAuxC + *	
32		Ch2 RxAuxC/TxAuxC - *		66		Ch4 RxAuxC/TxAuxC - *	
33		Ch2 RxSp/TxSp + *		67		Ch4 RxSp/TxSp + *	
34		Ch2 RxSp/TxSp - *		68		Ch4 RxSp/TxSp - *	

***** These signals only present on the SIO4BX-SYNC. They are reserved on the SIO4B-SYNC.