General Standards Corporation

High Performance Bus Interface Solutions

CCVPX-16AI32SSC1M

32-Channel, Differential, 16-Bit Simultaneous Sampling; Conduction-Cooled VPX Analog Input Board

With 1.0MSPS Sample Rate per Channel, Time-tagging, Low-latency access, and Front-Panel I/O

Features

- **32 Differential analog inputs with dedicated 1.0MSPS 16-Bit ADC per channel**
- **Sampling rates to 1.0MSPS per channel**
- **Simultaneous sampling of all inputs; Minimum data skew**
- **Software-Selectable Input ranges: ±10V, ±5V, ±2.5V or ±1.25V**
- **Standard conduction-cooled 3U VPX form Factor**
- **Front-Panel system I/O access**
- **Sync and clock I/O support external control and multiboard configurations**
- ***Time Tagging* attaches time information to each input data value**
- ***Low Latency* provides 32 registers that duplicate the most recent samples from all channels**
- Increased throughput capacity with local data packing
- Continuous, burst and single-sample clocking modes
- Hardware sync I/O for multiboard operation
- 1 MByte FIFO data buffer; 512 K-Samples in packed-data mode.
- 2-Channel DMA engine
- Conforms to PCI Express Specification revision 1.0a; x1 Link operating at 2.5Gbps
- Sample rate controlled by internal rate generators, by software triggering, or externally
- On-Demand internal Autocalibration of all channels

Typical Applications

✓ High-Density Analog Inputs	✓ Industrial Robotics	✓ Acoustic Sensor Arrays
✓ Analog Event Capture	✓ Crash Analysis	✓ Dynamic Test Systems

--- PRELIMINARY ---

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Functional Description

The conduction-cooled CCVPX-16AI32SSC1M analog input board provides 32 precision 16-Bit analog input channels on a standard 3U VPX module. All 32 inputs can be sampled simultaneously at rates from zero to 1MSPS, and the input range can be software-selected as ±10V, ±5V, ±2.5V or ±1.25V. Each channel contains a dedicated 16-Bit sampling ADC, a differential input amplifier, and selftest input switches. Converted input data is available to the host bus through a 1-MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing, or data can be accessed through low-latency data registers. Selectable Time Tagging attaches time information to each input data value. The board supports standard conduction-cooling.

Inputs can be sampled in groups of 2, 4, 8, 16 or 32 channels; or any contiguous channel group can be selected for sampling. Triggered bursts are supported. The sample clock can be generated from an internal rate generator, or by software, or by external hardware.

On-demand autocalibration determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

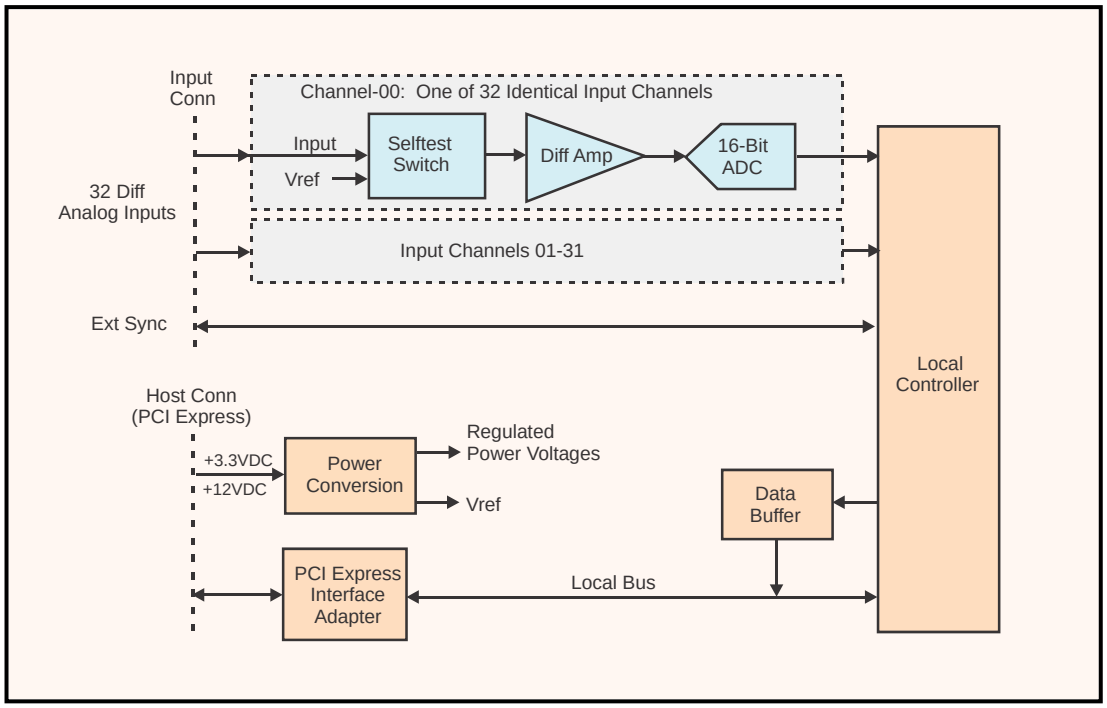

Figure 1. CCVPX-16AI32SSC1M; Functional Organization

This product conforms to the VPX baseline standard ANSI/VITA 46.0-2007 (R2013). System connections are made at the front panel through a high-density front-panel I/O connector. Power requirements consist of +12VDC and +3.3VDC in compliance with the VPX specification, and operation over the specified temperature range is achieved with standard conduction cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions, and with differential processing deselected

Input Characteristics:

Configuration:	32 differential analog input channels. 16-Channel version available.
Voltage Ranges:	Software configurable as ±10V, ±5V, ±2.5V or ±1.25V fullscale
Input Impedance:	2.0 Megohms typical, line-line. 1.0 Megohms line-ground..
Bias Current:	100nA maximum.
Common Mode Rejection:	80dB on ±10V range; 85dB on ±1.25V range; typical, DC-50kHz
Min/Max Input Levels for rated performance:	±11V
Crosstalk Rejection:	85dB typical, DC-50kHz
Input Noise:	0.4mVRMS, ±10V Range; 0.15mVRMS, ±2.5V Range; typical, 0.01-250kHz
Overvoltage Protection:	Sustained ±15 Volts with power removed; ±30V with power applied

Transfer Characteristics:

Conversion Resolution:	16 Bits (0.0015 percent of FSR)
Sample Rate:	Zero to 1,000 KSPS per channel
Input Bandwidth (-3dB):	DC to 400 kHz typical
Channels per Sample:	1-32

DC Accuracy: (Maximum composite error after autocalibration)

Range	Zero-Input	Fullscale
±10V	± 1.5mv	± 2.8mv
±5V	± 1.4mv	± 2.5mv
±2.5V	± 1.1mv	± 1.8mv
±1.25V	± 0.9mv	± 1.6mv

Integral Nonlinearity:	±0.008 percent of FSR, maximum
Differential Nonlinearity:	±0.004 percent of FSR, maximum

Analog Input Operating Modes and Controls

Input Data Buffer:	FIFO; 1 Megabyte. 256 K-Samples in normal (16-Bit) mode; 512 K-samples in packed-data mode. A 'Low-Latency' array of 32 data registers is available in addition to the FIFO buffer.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock. Continuous, Burst and Single-Sample Clocking Modes.
Rate Generator:	Two rate generators provide sample rates from 0.016-1,000,000 sample clocks per second, by dividing the local master clock to the sample rate. (The standard master clock frequency is 64MHz. See ordering information for custom frequencies.)
External TTL Sync, Clock:	Bidirectional TTL lines; available through the I/O connector, or through a 6-pin Sync-I/O connector located on the back of the board.
Input Data Format:	Nonpacked Mode: 16-Bit data word plus single-bit Channel-00 tag. Packed Mode: Lword sync code followed by packed channel data. Even-numbered channels occupy lower word (D00-15), odd channels occupy upper word (D16-31).
Data Format:	Selectable as offset binary or two's complement.
Low Latency:	In addition to the FIFO buffer, 32 data registers are directly accessible for minimum latency.
Time Tagging:	48-Bit 1-microsecond time stamping ('tagging') and windowed burst triggering.

Host Bus Compatibility:

Conforms to VPX VITA 46.0.
Also conforms to PCI Express Specification revision 1.0a; x1 Link operating at 2.5Gbps.
DMA transfers as bus master with two DMA channels.

Power Requirements:

+3.3VDC ±0.2 VDC, 1.4 Amps typical, 1.6 Amp maximum.
+12VDC ±0.4 VDC, 0.5 Amps typical, 0.6 Amps maximum
Total power consumption:10.0 Watts typical, 12.5 Watts maximum.

Mechanical Characteristics

Height: 18.8mm (0.74 in)
Depth: 170.6 mm (6.717 in)
Width: 100.0 mm (3.937 in)
Shield: Side-1 is protected by an EMI shield.
Thermal transfer rails are provided for conduction cooling.

Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +80 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating and Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Standard conduction cooling thermal interfaces.

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C", as indicated below.

For example, model number CCVPX-16AI32SSC1M-32-64M-0 describes a board with 32 input channels, a standard 64.000MHz master clock frequency, and no custom features.

All versions provide time-tagging and low-latency functions as standard features.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	32 Channels	A = 32
	16 Channels	A = 16
Master Clock Frequency:	64.000 MHz (Standard)	B = 64M
	Specify custom frequency; 64-66 MHz *	B = (Custom frequency)M
Custom Feature	No custom features	C = 0

* Frequencies other than the standard frequency will cause proportionate variations in the sample rate.

System Interface Connector

Table 1. System I/O Connector Pin Functions

Pin	Signal	Pin	Signal
43	INPUT RTN	---	---
42	INPUT RTN	85	INPUT RTN
41	INP 00 LO	84	INP 00 HI
40	INP 01 LO	83	INP 01 HI
39	INP 02 LO	82	INP 02 HI
38	INP 03 LO	81	INP 03 HI
37	INP 04 LO	80	INP 04 HI
36	INP 05 LO	79	INP 05 HI
35	INP 06 LO	78	INP 06 HI
34	INP 07 LO	77	INP 07 HI
33	INPUT RTN	76	INPUT RTN
32	INP 08 LO	75	INP 08 HI
31	INP 09 LO	74	INP 09 HI
30	INP 10 LO	73	INP 10 HI
29	INP 11 LO	72	INP 11 HI
28	INP 12 LO	71	INP 12 HI
27	INP 13 LO	70	INP 13 HI
26	INP 14 LO	69	INP 14 HI
25	INP 15 LO	68	INP 15 HI
24	INPUT RTN	67	INPUT RTN
23	INP 16 LO	66	INP 16 HI
22	INP 17 LO	65	INP 17 HI
21	INP 18 LO	64	INP 18 HI
20	INP 19 LO	63	INP 19 HI
19	INP 20 LO	62	INP 20 HI
18	INP 21 LO	61	INP 21 HI
17	INP 22 LO	60	INP 22 HI
16	INP 23 LO	59	INP 23 HI
15	INPUT RTN	58	INPUT RTN
14	INP 24 LO	57	INP 24 HI
13	INP 25 LO	56	INP 25 HI
12	INP 26 LO	55	INP 26 HI
11	INP 27 LO	54	INP 27 HI
10	INP 28 LO	53	INP 28 HI
9	INP 29 LO	52	INP 29 HI
8	INP 30 LO	51	INP 30 HI
7	INP 31 LO	50	INP 31 HI
6	INPUT RTN	49	INPUT RTN
5	DIG RTN	48	DIG RTN
4	DIG RTN	47	CLOCK RST INP
3	DIG RTN	46	REF CLK INP
2	DIG RTN	45	CLOCK I/O [1] or SAMP CLK INP [2]
1	DIG RTN	44	SYNC I/O [1] or SAMP CLK OUT [2]

[1] Default configuration. Not software-configured for time tagging.

[2] If software-configured for time tagging.

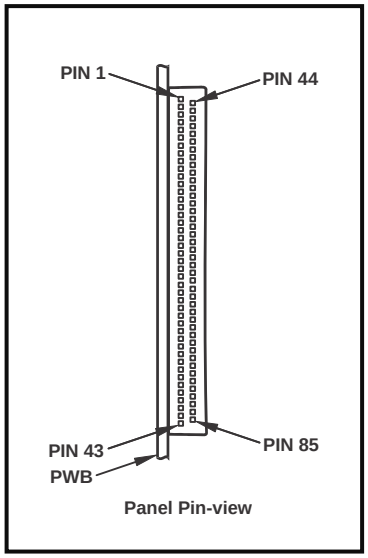

Figure 2. System I/O Connector

System I/O Mating Connector:
Omnetics # MNPO-85-DD-N-EJS-C, dual-row, straight tail.
(Assembled cables available)

Table 2. Sync-I/O Pin Functions

SYNC-I/O Conn Pin	Signal
1	DIG RTN
2	AUX CLOCK
3	DIG RTN
4	AUX SYNC
5	DIG RTN
6	Reserved. Connect to INPUT RTN or leave disconnected.

Recommended Sync-I/O mating connector: Molex# 51146-0600.