General Standards Corporation
High Performance Bus Interface Solutions

PMC66-24DSI6LN4AO

10-Channel Analog I/O PMC

Six Simultaneous, 24-Bit Delta Sigma, Input Channels, With Four 16-Bit Output Channels, and Byte-Wide Digital I/O Port

Features Include:

- ***Advanced component upgrade***, with original ADADIO functionality and I/O connector pinout.
- 6 Analog input channels; 24-Bit ADC per channel; Delta-Sigma converter.
- 4 Analog output channels; 16-Bit DAC per channel.
- 8-Bit Bi-directional Digital Port with two auxiliary control lines.
- Simultaneous analog input sampling; with Linear Phase Antialias filtering.
- Analog input sample rates adjustable up to 100ksps. (200ksps option available.)
- 256K-Sample analog input FIFO buffer.
- Supports Continuous and Triggered-Burst input modes.
- Analog outputs disconnect from system under software control.
- Simultaneous updating of outputs with external hardware strobe, software strobe or internal rate generator.
- Analog output data rates to 250K Samples per second or more per channel, host dependent.
- 33MHz/66 MHz, 32-Bit PCI support, with universal 5V/3.3 signaling.
- Single-width PMC form factor.
- Extended temperature range available.
- VxWorks™ Driver available.

Applications:

- ✓ Supervisory Control Systems
- ✓ Data Acquisition Systems
- ✓ Research Instrumentation
- ✓ Automatic Test Equipment
- ✓ Simulators and Trainers
- ✓ Process Control

****** PRELIMINARY ******

Rev: 070921

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Overview:

The PMC66-24DSI6LN4AO is a single-width PMC module which contains six 24-Bit A/D converters, four 16-bit D/A converters, and all supporting functions necessary for adding flexible analog I/O capability to a PMC host. All analog input and output system connections are made through a single 68-pin subminiature-D front-access I/O connector. The analog outputs can be internally disconnected from the system I/O connector under software control.

Each analog output channel is accessed through an independent 16-bit data register in PCI memory space. ADC conversion data are read by the bus through an analog input FIFO buffer. An auxiliary digital port contains eight bits of bi-directional data and two control lines, and is controlled through a single register.

Communication with the host PCI bus is provided by a PCI Interface Adapter which furnishes a 32-bit local bus for exchanging information between the FIFO buffers, the adapter, and the Local Controller. All internal operations are managed by the Local Controller.

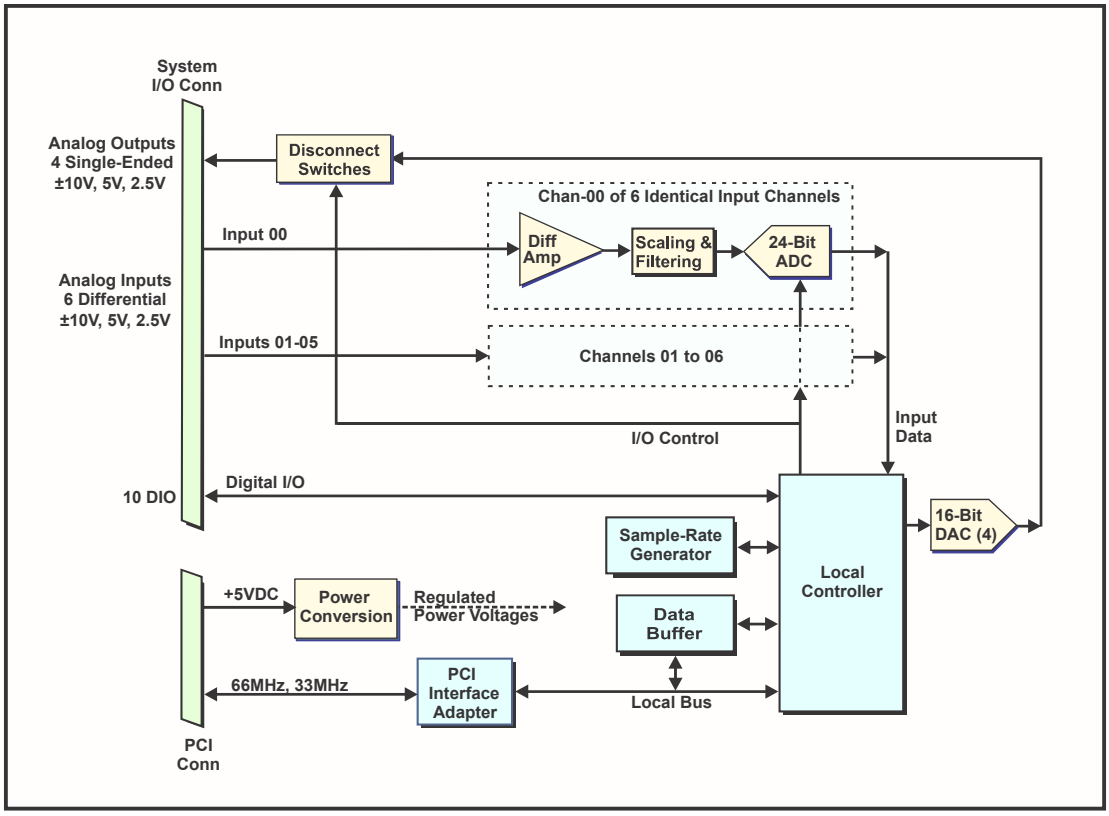

Figure 1. PMC88-24DSI6LN4AO Analog I/O Board, Simplified Functional Diagram

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System input/output connections are made at the front panel through a high-density 68-Pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating conditions

ANALOG INPUT CHANNELS

Input Characteristics:

Configuration:	6 analog input channels; software-selected as differential or single-ended. 4-Channel version available.
Voltage Ranges:	Factory configured as ±10, ±5, or ±2.5Volts.
Input Impedance:	1.0 Megohms in parallel with 20 pF; 2.0 Megohms line-to-line
Input Coupling:	Selectable as either AC-coupled or DC-coupled. AC coupling provides lower noise.
CMRR	Common Mode Rejection Ratio = 60dB to 50 Hz typical
Common Mode Range:	±11.0 Volts; with zero input signal level
Remote Ground Sensing:	All single-ended inputs are measured relative to the external return, which is isolated from the internal analog return by approximately 200 Ohms.
Overvoltage Protection:	±30 Volts with power applied; ±15 Volts with power removed
External Trigger Input:	TTL level, active LOW

Transfer Characteristics:

Resolution: 24 Bits

Sample Rate: 2,000 to 200,000 samples per second per channel

Oversampling Factor: 2-50ksps: x128; 50-100ksps: x64; 100-200ksps: x32

DC Offset: ±50mV max; Inputs connected to input return.

Gain Accuracy: ±2dB within passband

Passband (0.2dB):

Sample Rate:	Typical, DC Coupling*
2-50ksps:	DC to 0.47 Fsamp
50-100ksps:	DC to 0.46 Fsamp
100-200ksps:	DC to 0.24 Fsamp

***-0.13dB low end of passband is Fsamp/2400 in AC-coupled mode. E.g.: 20Hz if Fsamp=48KSPS.**

Passband Ripple: ±0.06dB maximum

Stopband:

Sample Rate:	Threshold	Rejection
2-50ksps:	0.58 Fsamp	100dB
50-100ksps:	0.68 Fsamp	95dB
100-200ksps:	0.78 Fsamp	100dB

Phase Skew: Typically less than 55ns (0.1-Degree for Fsig = 5kHz), with Fsig/Fsamp <0.35; channel-channel (board-board for multiboard configurations), excluding noise, with high-frequency image filter.

Antialias Filtering: Each ADC provides linear-phase digital antialias filtering as indicated for Passband and Stopband. A 270kHz lowpass analog image filter in each channel suppresses images from the digital filter. Optional alternative image filter frequencies are available, and should be selected to be well above the expected passband.

Dynamic Range:

Input Range	Dynamic Range*
±10V	100dB
±5V	94dB
±2.5V	88dB

*Typical to 50KSPS. Degrades by 15dB from 50KSPSto 200KSPS.

SINAD: 98dB typical to Fsig=20kHz and sample rates to 50KSPS.

Interchannel Crosstalk: -100dB typical to 50kHz

Analog Input Operating Modes and Controls

Input Sampling Mode:	Continuous Conversion Mode (Default): Analog inputs are converted continuously at the selected conversion rate. Inputs are selected as differential or single-ended. Burst Scan Mode: A single conversion of selected channels is initiated by an external hardware trigger or by a software trigger.
Sample Rate Generator:	An internal PLL rate generator provides sample rates from 2.0 KSPS to 200 KSPS. The frequency of the generator is controlled by the ratio of two 10-Bit integers, and has a setting accuracy is 25 PPM.
Active Channels:	Software selected from 1 to 6 channels. Conversion data from active channels appear in the analog input buffer. Active channels are contiguous, beginning with Channel-0 and proceeding upward to the highest active channel number.
Data Buffer:	FIFO buffer with a capacity of 256K samples.
Buffer Flags:	Buffer threshold flag.
Data Format:	Software selected as offset binary or two's complement format
Multiboard Synchronization:	A single initiator card can be used to trigger synchronized conversions in up to three target cards through a TTL interface.

ANALOG OUTPUT CHANNELS

Output Characteristics:

Configuration:	Four single-ended output channels
Voltage Ranges:	Factory configured as ±10, ±5, or ±2.5Volts. (Same range as inputs)
Output Resistance:	2.0 Ohms, maximum if outputs are enabled; 33 kOhms to ground if outputs are disabled
Output protection:	Withstands sustained short-circuiting to ground. Also withstands overvoltage transients to ±40 Volts through 80 Ohms for 10 milliseconds.
Load Current:	±5 mA maximum; ±2 mA recommended for minimum crosstalk and line loss
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Noise:	1.4 mVrms, 10Hz-10MHz

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Maximum Sample Rate:	Minimum of 250K samples per channel. Useable rate is host-dependent.
DC Accuracy, Line-Line: (No-load)	Range ±10V: Midscale Accuracy ±4.1mv, ±Fullscale Accuracy ±6.3mv Range ±5V: Midscale Accuracy ±3.2mv, ±Fullscale Accuracy ±4.9mv Range ±2.5V: Midscale Accuracy ±2.0mv, ±Fullscale Accuracy ±3.5mv
Settling Time (0.01%):	50uS => No filter (~70lHz) 0.9mS => 4kHz flter 3.0mS => 1.2kHz Flter
Crosstalk Rejection:	75 dB minimum, DC-1000Hz
Integral Nonlinearity:	±0.007 percent of FSR, maximum
Differential Nonlinearity:	±0.003 percent of FSR, maximum
External Strobe Input:	TTL level, active LOW

Analog Output Operating Modes and Controls

Output Access::	Direct write to register, unbuffered.
Output Strobing:	Outputs can be clocked (strobed) from any of these sources: • Internal rate generator, • External hardware clock, • Software clock, • Automatically (Self clocking in Sequential clocking mode).
Output Enabling:	Analog outputs are connected to the system I/O connector if analog outputs are enabled, or are disconnected if analog outputs are disabled.
Data Registers:	16-bit data register per output channel
Data Format:	Software-selected as offset binary or two's complement format

DIGITAL I/O PORT

Configuration:	8 bidirectional data lines and two control lines. One control line is a dedicated output; the other control line is a dedicated input. All lines implement standard TTL logic levels.
Data and Control Register:	Single 32-bit register. Maximum loading ±20mA. All lines pulled up internally to +5V through 33K.
Transfer Rate:	Typically 10^6 transfers per second, host-dependent

PCI INTERFACE

Compatibility: Conforms to PCI Specification 2.3; D32, 33/66MHz, Universal 3.3V/5V signaling.
Supports "plug-n-play" initialization.
Provides multifunction interrupt.
Supports DMA transfers as bus master; block and demand modes.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Power Requirements

+5VDC ±0.2 VDC at 1.5 Amp, maximum, 1.4 Amp typical

Maximum Power Dissipation: 6.5 Watts, Side 1
1.0 Watt, Side 2

Physical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side 1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range

Standard Range:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Range:	Operating: -40 to +80 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	Operating and Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM minimum air flow

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For extended temperature operation, add the suffix "-ET" at the end of the part number.

For example, model number "**PMC66-24DSI6LN4AO-6-4-2.5-270K-ET**" describes a board with six input channels, four output channels, the ±2.5V range, standard image filter frequency, and extended temperature operation.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	Six	A = 6
	Four	A = 4
Number of Output Channels	Four	B = 4
	None	B = 0
Input/output Range	±10 Volts	C = 10
	±5 Volts	C =5
	±2.5 Volts	C = 2.5
Image Filter Frequency	Standard 270kHz filters	D = 270
	Custom frequency	D = CF (kHz)

Table 1. System Connector Pin Functions

P5A	
PIN	SIGNAL
1	OUTPUT RETURN
2	OUTPUT CHANNEL 00
3	OUTPUT RETURN
4	OUTPUT CHANNEL 01
5	OUTPUT RETURN
6	OUTPUT CHANNEL 02
7	OUTPUT RETURN
8	OUTPUT CHANNEL 03
9	INPUT RETURN
10	INPUT RETURN
11	INPUT CHANNEL 00 LO (-)
12	INPUT CHANNEL 00 HI (+)
13	INPUT CHANNEL 01 LO (-)
14	INPUT CHANNEL 01 HI (+)
15	INPUT CHANNEL 02 LO (-)
16	INPUT CHANNEL 02 HI (+)
17	INPUT CHANNEL 03 LO (-)
18	INPUT CHANNEL 03 HI (+)
19	INPUT CHANNEL 04 LO (-)
20	INPUT CHANNEL 04 HI (+)
21	INPUT CHANNEL 05 LO (-)
22	INPUT CHANNEL 05 HI (+)
23	NO CONN*
24	NO CONN*
25	NO CONN*
26	NO CONN*
27	VREF RETURN
28	VREF ADJUST REFERENCE
29	VREF RETURN
30	VREF REMOTE ADJUST
31	VREF RETURN
32	RANGE VREF
33	VREF RETURN
34	VREF RETURN

P5B	
PIN	SIGNAL
1	DIGITAL RETURN
2	INPUT TRIGGER
3	DIGITAL RETURN
4	INPUT TRIGGER READY
5	DIGITAL RETURN
6	OUTPUT STROBE
7	DIGITAL RETURN
8	OUTPUT STROBE READY
9	DIGITAL RETURN
10	I/O DATA 00
11	DIGITAL RETURN
12	I/O DATA 01
13	DIGITAL RETURN
14	I/O DATA 02
15	DIGITAL RETURN
16	I/O DATA 03
17	DIGITAL RETURN
18	I/O DATA 04
19	DIGITAL RETURN
20	I/O DATA 05
21	DIGITAL RETURN
22	I/O DATA 06
23	DIGITAL RETURN
24	I/O DATA 07
25	DIGITAL RETURN
26	I/O CONTROL INPUT
27	DIGITAL RETURN
28	I/O CONTROL OUTPUT
29	DIGITAL RETURN
30	DIGITAL RETURN
31	DIGITAL RETURN
32	DIGITAL RETURN
33	DIGITAL RETURN
34	DIGITAL RETURN

*** Open circuit. No internal connection.**

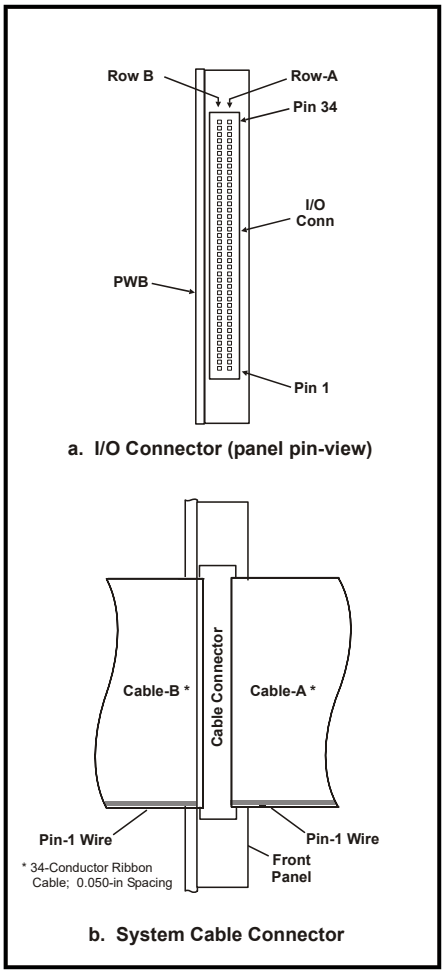

Figure 2. System I/O Connector

System Cable Mating Connector:
68-pin 0.050" Subminiature connector: with metal shield: AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:** Amp # 787170-7